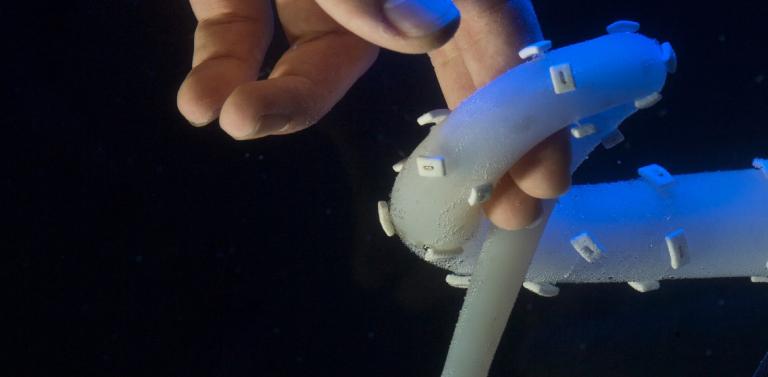
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PUBLISHER

André Rousselot

+32 27400053

andre.rousselot@eetimes.be

EDITOR-IN-CHIEF

Julien Happich

+33 153907865

julien.happich@eetimes.be

EDITORS

Philip Ling

+44 1622746580

phil.ling@eetimes.be

Christoph Hammerschmidt

+49 8944450209

chammerschmidt@gmx.net

CONTRIBUTING EDITORS

Paul Buckley

+44 1962866460

paul@activewords.co.uk

Jean-Pierre Joosting

+44 7800548133

jean-pierre.joosting@eetimes.be

CIRCULATION & FINANCE

Luc Desimpel

luc.desimpel@eetimes.be

ADVERTISING PRODUCTION & REPRINTS

Lydia Gijsegom

lydia.gijsegom@eetimes.be

ART MANAGER

Jean-Paul Speliers

ACCOUNTING

Ricardo Pinto Ferreira

REGIONAL ADVERTISING REPRESENTATIVES

Contact information at:

http://www.electronics-eetimes.com/en/about/

sales-contacts.html

EUROPEAN BUSINESS PRESS SA

144 Avenue Eugène Plasky 1030 Brussels - Belgium

Tel: +32 (0)2 740 00 50

Fax: +32 (0)2 740 00 59

www.electronics-eetimes.com VAT Registration: BE 461.357.437

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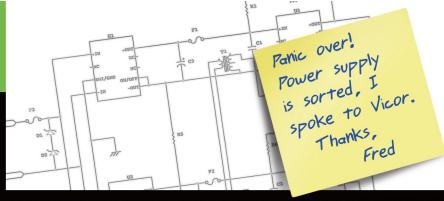
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Betting on liquid TSV processes for 3D integration

By Julien Happich

A 2001 SPIN-OFF FROM CEA-SACLAY, tenyear old French company Alchimer has grown from a chemistry research lab to become the credible provider of a cost-saving wet alternative to dry through-silicon via (TSV) processes. Promoting its patented electrografting (eG) and chemical grafting (cG) technologies, the company wants its share of the TSV and interposer IC packaging business and has already secured significant licensing agreements with Asian equipment manufacturers.

Meeting with EETimes Europe in Paris, Steve Lerner, Alchimer's CEO made pretty bold statements about the state of the industry on 3D packaging and IC integration. When asked about the need for a new process flow or the limitations of current dry processes in use for the elaboration of TSVs, Lerner turned ironic "All the major players in the TSV industry are focusing on how to solve the problems inherent to directional deposition techniques such as physical vapour deposition (PVD), ionized PVD (iPVD), or chemical vapour deposition (CVD), just so they can keep selling their inadequate tools".

"The tools that are used to build TSVs today were conceived for planar jobs", he argues, "and they all fall apart when it comes to tackling 3D integration with complex, highaspect ratio structures with recessed features". One example Lerner likes to put forward is the emergence of tapered TSVs at conferences and seminars, heralded as the best fix to circumvent the poor fill factors and sidewall scalloping effects achieved with dry process flows. "Why turn to tapered vias when all what you want is to connect two layers with a minimal copper footprint?" he questions, "That's wasted real estate". He remembers the days when Alchimer would present academic papers and concepts about the wet eG and cG technologies, enabling the deposition of highly-uniform isolation or barrier material layers for lining 3 micron diameter TSVs with true aspects ratios over 20:1. "Nowadays, with about 200 patents filed or pending, we are confronting the Goliaths of the dry process industry with an unpleasant truth about the limitations of their solutions, and certain boards of conference no longer find our presence relevant. We are fighting our way against deeply entrenched companies and somehow, it is as if we were trying to sell an electric car to



"Why turn to tapered vias when all what you want is to connect two layers with a minimal copper footprint?"

General Motors 20 years ago, they don't want to see a new technology steal the show." Lerner remarks. "We are also confronted with the Dilberts of this world", lerner notes with humour, "for every one engineer of the wet culture, there are a thousand Dilbert engineers of the dry culture who won't dare make a change for better, because we are still a fairly small company". Nowadays, 95% of Alchimer's customers are located in Asia, and this is where Lerner sees the 3D integration happening first in high volume production, with China being a strong technology investor. Asian companies are not as much risk-averse as US companies, which explains Alchimer's recent signing of a multilevel production collaboration agreement with South Korean chemical and equipment manufacturer KPM Tech that includes wet processing tools and materials for Alchimer's through-silicon via platform. Alchimer also licensed its technology to a MEMS consortium in North America.

What differentiates Alchimer is its lowtemperature wet approach, whereby mildly basic water-based chemistries are used to grow material layers directly on the silicon substrates or onto whatever chemically-compatible layer has been grown before, with strong chemical bonds. Each layer construction is reactant- and temperature-controlled for the chemical grafting process and reactant- and

potential-controlled for the electrografting process, growing from the bottom up, hence forming a highly conformal layer regardless of the structure complexity, in the range of 50 to 300nm in thickness. The term "grafting" refers to the strong chemical bonds that form at the molecular level between the substrate and the film being grown. "Alchimer's suite of AquiVia films covers the needs for isolation, barrier deposition and TSV copper fill at less than half the cost offered by current dry processes while being compatible with existing wafer-processing infrastructures." explains Lerner, "what's more, we don't tie the hands of designers with primitive geometry rules" he adds. Alchimer focuses on thin films because they are at a premium now, and this is where competition is, but Lerner also sees PCB manufacturers as the future market place since they can't always afford the expensive dry process equipment needed for fine interposer geometries. Initially, Alchimer didn't plan to get into the "copper fill" business, but then it realized it had the technology to fill copper vias in less than half the time required by competing processes, while drastically reducing the number of Chemical-Mechanical Polishing (CMP) steps that are usually needed to eliminate the excess of copper deposited with the typical successive dry processes. The company recently joined the Global Semiconductor Association (GSA) and hopes to be able to push packaging and interposer design rules more aggressively thanks to its innovative solutions. "Some big guys have already designed 3D-integrated packages that can't be done with dry processes" claims Lerner, "as soon as we can make some announcements and be taken more seriously, we'll be able to talk to foundries and maybe EDA companies too. To hit the nail further, Alchimer has just announced a new wet deposition process called AquiVantage, that provides metallization for interposer and via-last in 3D packaging for chip-to-board interconnect. The process provides concurrent wet deposition of TSV and front-side isolation, barrier, and copper fill/interposer redistribution layers (RDLs), while eliminating CMP and dry deposition steps. On the backside, the AquiVantage process allows selective maskless growth of the on-silicon isolation layer, completely eliminating an entire expose/develop/etch/clean lithography process cycle. ■

News & Technology

PCIM tackles power efficiency from various angles

By Christoph Hammerschmidt

ENERGY EFFICIENCY HAS become the focus of politicians, managers - and, of course, engineers. The PCIM trade fair in Nuremberg gave us some hints about which efficiency improvements are enabled by technology and how we can progress further.

Countermeasures can be defined against power losses in electronic systems, operating at several levels - the control strategies, the circuit topologies for converters, and inverters. Strategies aiming at better efficiency include replacing electromechanical parts with electronic switches, replacing traditional and relatively "dumb" control technologies such as triac-based phase angle control schemes by smarter variable-frequency controls with energy recuperation or replacing "always on" mechanical control elements (such as power steering in the car) by electric elements which are activated only on demand.

Clearly, this year's PCIM exhibition and congress program focused on the component level. For instance, Infineon introduced a new generation of its CoolMOS high-voltage MOSFETs. The CFD2 product family features a breakthrough voltage of 650V, 50V more than its predecessors of the CFD family, and an integrated fast-body diode. According to product line manager Jan-Willem Reynaerts, the new products boast a smoother switching behaviour and lower EMI radiation compared to their predecessors, which results in better energy efficiency. In particular at low loads, the efficiency has been improved. Optimized for resonant switching topologies, Infineon plans to market the new devices for applications such as solar power inverters, compute servers, lighting and telecommunications.

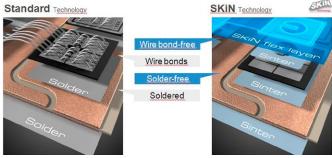
Power semiconductor and module manufacturer Semikron showed an interconnection technology for power modules which according to the company permits better thermal and electrical chip statistics: instead of conventional wire bonding and solder connections, the new SkiN technology is based on a flexible interconnection layer and sinter layers for better thermal conduction. For instance, the continuous sinter layer allows for 25% higher surge currents than a comparable

wire-bond design, explained Thomas Grasshoff, head of Semikron's product management. The sinter layers offer 30 percent lower thermal resistance of only o.65 Kelvin per Watt. This improvement translates

into an increase in current density by a factor of 2 to 3 A/cm². As a consequence of the better thermal management, SkiN modules will offer ten times higher power cycling compared to standard modules, Grasshoff said. The sinter technology could provide a migration path to the SiC and GaN power semiconductors of the future as it can be used at the higher junction temperatures (over 200°C) that are typically associated with these semiconductors.

Next-generation semiconductor materials such as Silicon carbide (SiC) and Gallium nitride (GaN) were a major topic at the fair, and even more so at the associated congress. A panel discussion was dedicated to the topic of wide bandgap semiconductors and current developments. According to PCIM conference director Leo Lorenz (who also is senior principal of Infineon and president of the European Center for Power Electronics, ECPE), the industry is currently in the home stretch to the commercial production of a SiC JFET. The product roll-out can be expected before the end of this year.

Infineon, by the way, won't be the first company to offer SiC-based power transistors. SemiSouth Inc. already reached industrialscale production. At PCIM the company introduced a SiC device that switches 1200V and features an RDS(on) of 45 mOhms. "Silicon carbide permits significantly higher switching frequencies than IGBTs at just one tenth of the power loss", explained SemiSouth European Director Dieter Liesabeths. While a SiC transistor currently costs four times the price of a comparable IGBT, it enables design engineers to significantly reduce system costs. "For instance, you can build power supplies with a switching frequency of 80 kHz, compared to 20 kHz in a conventional power supply. Thus, you will be able to reduce the size of the



Semikron's SKiN power module packaging technology permits significantly higher power density.

transformer by one third which already offsets the higher price for the SiC transistor."

The gallium nitride technology however, regarded by some semiconductor masterminds as an even more efficient alternative to SiC, is still several years away - for a number of reasons. "The sapphire substrate used for GaN semiconductors permits only lateral structures", Lorenz said. "But for power devices you need vertical transistor structures".

The materials are just one variable of the equation for design engineers willing to tackle efficiency. Another popular strategy to improve power efficiency is to reducing standby power consumption by means of novel electronic switches. While standby power reduction for stereo equipment, TV sets or washing machines is not a new topic, more affordable components will help drive down unwanted power consumption when the appliances are not in use. In order to facilitate the transition to lower power standby supplies, Taiwanese semiconductor manufacturer Power Integration launched two new members of its LinkZero-AX family, an integrated offline switching IC product family that enables designers to achieve zero Watts of standby energy consumption in auxiliary power supplies. The chips feature a power-down mode that effectively turns off the auxiliary power supply when the end product is idle or in standby. The power-down mode is triggered by a signal accessible to a microcontroller, shutting down the internal switch control circuits completely. However, while in power-down mode, the bypass pin remains regulated, allowing the LinkZero-AX IC to be awakened with a reset pulse or button press. At PCIM, Power Integration introduced two new members of this product family which can control main output power output of up to 6.5W.

Android aims for greater unity, **USB** support

By Rick Merritt



AT ITS ANNUAL DEVELOPER CONFERENCE, Google outlined plans to integrate separate versions of Android, and to extend the software to support USB and home automation.

Support for tablet, smartphone and television versions of Android will come together in a so-called Ice Cream Sandwich version of the software to be released as open-source code in the fourth quarter. The current Honeycomb version 3.0 for tablets, and a 3.1 upgrade due within weeks, will not be made available as open source, but their features will be rolled into the code released at the end of the year.

With the latest announcements, it becomes clear that only a handful of top-tier OEM partners will have Honeycomb tablets this year. The rest of the industry will have to wait for the release of Ice Cream Sandwich to power a broader set of tablets in 2012.

Meanwhile, GoogleTV client software will continue to be a sepa-

rate variant of Android. This summer, Google will make available a new version of that code based on Honeycomb 3.1. Apps developed for that version will become available in a new GoogleTV section of the public Android apps market online.

If it all sounds a bit confusing, it is. Google has released eight Android versions in two and a half years. Android is currently being used on 310 different devices and was activated on 100 million phones in 2011, with activations tracking at 400,000 a day, Hugo Barra, director of Android product management, said in a Google I/O keynote.

In a fireside chat with Google's Android managers, one developer complained that fragmentation of the code base is becoming "a nightmare for developers, especially game developers," drawing supporting applause from an audience of several hundred peers.

"We want one OS that runs everywhere, and we want to insulate developers from differences in devices," said Mike Cherod, a Google developer working on Ice Cream Sandwich, alluding to tools in the works that will more easily support a single application on displays of different sizes.

Separately, Google announced an alliance of more than a dozen partners that will define a standard plan for upgrading Android devices in the field. The group includes AT&T, HTC, LG, Motorola, Samsung, Sony Ericsson, Verizon and Vodafone.

The effort aims to help users keep pace with Google's fast release cycles. The group has pledged to make any Android upgrades available on devices in the field for the first 18 months after their purchase.

At the end of the day, Android is a kind of hybrid—a planned set of open-source releases by a Google team moving as fast as it can to respond to its community of OEMs, developers and users. But it is neither 100 percent community-driven nor entirely open-source, Andy Rubin, head of Android at Google, said during a press briefing.

"In my opinion, a community process doesn't work when you are adding APIs, because it's hard to tell what's a release or a beta. Someone could take an early version of code and build devices with it that would not be compatible," Rubin said.

"So we decided to use scheduled releases going forward, because part of our job is to make sure [the code and products based on it] stay together," said Rubin. "We still accept submissions from the community, but it comes out in a much more contro lled way."

Under the hood, the plumbing is sometimes messy, with many issues still being worked on, Google developers said during the Android fireside chat. For instance, the company aims to rewrite parts of its core scheduler to improve audio latency, which it admits is not up to the level of Apple's iOS.

"We hope to do something in Ice Cream Sandwich" to address the audio latency problem, said David Sparks, technical lead for media frameworks on Android. "Some drivers and chip sets can add a hundred milliseconds of latency today. But we know we also have problems in how we schedule low-latency audio tasks; that's our biggest issue."



























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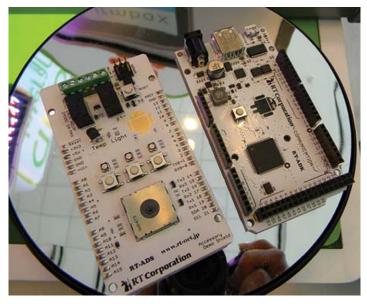
Microchip's Android USB board will ship in June for \$79.

USB support for Android

Even as Google labors to ratchet down the complexity of Android releases, it is aggressively extending the software to support accessories and home automation. In that respect, Google's message has changed.

In its early days, Android was focused solely on the mobile phone. Now the software is extending its reach to tablets, TVs and a growing set of other devices, Google execs are quick to note.

Android will support USB for the first time in the next version of the software for tablets (Honeycomb 3.1) and the next smartphone



RT's Android USB boards will sell together for \$380.

version (Gingerbread 2.3.4). The support includes a new Open Accessory API that includes USB 2.0 support libraries from Google.

Android is unusual in that it is defined as a device, not a host environ-ment under Linux. Thus Android USB accessories will technically be USB hosts. The Google libraries aim to smooth over that distinction for developers. The device/host situation means Android USB accessories will not be able to get power over USB from Android handsets or tablets. Google is not developing support for USB 3.0.

Google, Microchip and Japan's RT Corp. announced hardware

developer kits for building Android USB accessories based on the popular Arduino board. The Microchip board uses a MIPSbased processor and will be available by June for \$79. Robotics developer RT showed an Arduino board and a separate sensor board; it will sell the two as a pair for \$380.

Google said it will also release support for Android accessories using Bluetooth in the future. A Google manager contrasted the new Android peripherals market to the tightly controlled one maintained by Apple for its iPhone and iPad.



The \$35 LED bulb from Lighting Science builds inlow-cost wireless networking for Android.

"There will be no NDAs or fees, and no approval processes to build accessories, so go get started," said Android product director Barra.

Separately, Google announced Android@Home, an initiative to link Android devices to a broad range of home appliances and home automation devices over Wi-Fi or a new, low-cost wireless home control network. Lighting Science (Satellite Beach, Fla.), an LED light and switch maker, said that by the end of year it will release \$35 LED light bulbs and gateways that can be controlled wirelessly by Android devices.

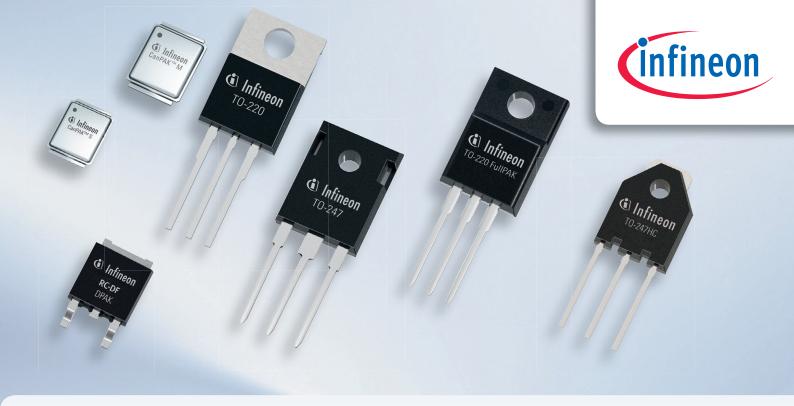
Google is expected to release open-source code late this year for a 915-MHz wireless mesh protocol that will be a low-cost alternative to Zig-Bee or Z-Wave. It could require as little as 16 kbytes of RAM and 32 kbytes of flash, enabling a 30 percent lower bill of materials than for ZigBee Pro.

The Google protocol will enable frequency hopping and ride on top of the 6LoWPAN (IPv6 over Low-Power Wireless Personal Area Networks) spec from the Internet Engineering Task Force.

The Android@Home initiative includes a hardware reference design called Project Tungsten for controlling home media systems. Google demonstrated a Tungsten box linked to the Web; waving a device equipped with a near-field communications link controls a stereo or enables the purchase and startup of an Internet audio stream.

"This combination of new cloud services, software and devices enables a whole universe of applications," said the Google developer who gave the demo.

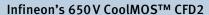
The Android@Home software and details of its wireless network support will be released late this year.

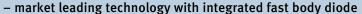


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IBM and ETH Zurich open the Binnig and Rohrer Nanotechnology Center

By Julien Happich

CELEBRATING ITS 100TH ANNIVERSARY

of existence as well as commemorating the 30th anniversary of the scanning tunnelling microscope (STM) invented by Nobel laureates Gerd Binnig and Heinrich Rohrer at the IBM Zurich Research Lab in 1981, IBM opened the Binnig and Rohrer Nanotechnology Center on its research campus near Zurich.

The two scientists, present during the opening, were deeply moved to have a research center named after them. The facility, which was planned three years ago, represents a USD 60 million investment from IBM as well as an additional USD 30 million split between IBM's research partners for tooling and equipment. It is the centre piece of a 10-year strategic partnership in nanoscience between IBM and ETH Zurich (Swiss Federal Institute of Technology, Zurich) where scientists will research novel nanoscale structures and devices (roughly from 1 to 100 nanometers) to advance energy and information technologies.

With three floors above ground, over 950m2 of clean rooms have been laid out in the new building, designed flexibly to receive any type of processes and experiments for micro- and nanofabrication. A special area has also been accommodated for processing carbon-based materials and structures.

In the basement, six uniquely designed noise-free labs shield extremely sensitive experiments from external disturbances, such as vibrations, electro-magnetic fields, for example from nearby trains and cellphone towers, temperature fluctuations and acoustic noise. 8m below street level, the custom-made LED-lit labs are built directly on the bedrock and are designed to achieve a temperature stability of ΔT < 0.1° C/h thanks to a vertically controlled laminar air flow. The entire rooms (including doors, electric cabinets etc.) are clad with magnetic metal (NiFe) and noise-producing equipment such as pumps, transformers, or power supplies are housed in adjacent chambers. The tools are remotely operated from an external operating room to minimize human heat dissipation (around 100W) and the instruments and experiment tables are supported on a massive air-springsuspended and actively controlled concrete seismic blocks weighing between 30 and 68 tons each to reduce vibration levels below 500nm/s. The surrounding platforms are entirely de-coupled

for researchers to access the experiments without stepping on the seismic blocks. An active electromagnetic fields compensation performed by Helmholtz coil pairs in x, y and z dimensions ensures that electromagnetic fields are kept below 5nT AC or below 20nT DC.

The attenuation foam-covered walls maintain an acoustic noise level below 30dB. According to noise-free labs project leader Dr. Emanuel lörtscher, these noise-free labs have specifications that are several orders of magnitude better than other existing infra-



One of the noise-free labs in the basement. All feature vibration levels below 500nm/s and active electromagnetic fields compensation below 5nT AC.



The newly built four-floor Binnig and Rohrer Nanotechnology Center boasts over 950m² of clean rooms and 176m² of noise-free labs.

structures and thus are more protected from external disturbances.

IBM wants the Nanotechnology research center to become an open infrastructure, with no strings attached, offering bestin-class tools and equipment for talented researchers. The centre will host both joint and individual research projects, led by project-based users as well as by permanent researchers from ETH who will have part of their lab located on the IBM research campus. The intellectual property derived from the research will be shared on a case-by-case basis, depending on how much shared work and know-how is involved from both ETH Zurich and IBM research groups.

In its first year, about 30 researchers from ETH will be working at the Binnig and Rohrer Nanotechnology Center. Three ETH professors and their teams have already moved into the new building and will conduct part of their research in nanoscience there on a permanent basis.

In addition to these partnerships, IBM will also collaborate in the center with scientists from several Lithuanian universities under a five-year agreement that was signed in September 2010 with the Lithuanian Ministry of Economy and Ministry of Education and Science. This collaboration will focus on integrated photonics and novel photonic materials to create faster computers, improved solar technologies, and nanopatterning security tags for advanced anti-forgery technology.

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Rohde & Schwarz, Synopsys join forces to boost LTE hardware design

By Christoph Hammerschmidt

WITH THE LTE TECHNOLOGY market approaching the stage of mass production, the demand for design support solutions is increasing. This in particular holds true for the LTE Advanced technology. Measurement equipment maker Rohde & Schwarz and EDA software vendor Synopsys plan to get the ball rolling.

In a strategic collaboration, the companies plan to exchange technological knowhow which could enable design engineers to faster get their LTE and LTE Advanced designs done. At the same time, they will be able to verify their designs of base station, handset and dongle chipsets for the 4G mobile radio standard. The collaboration is

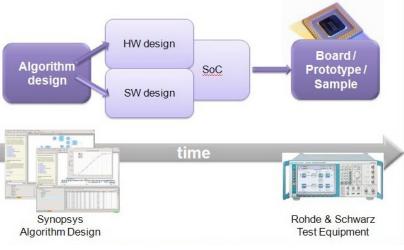
also aimed at the LTE Advanced standard for which no hardware is commercially available yet. The move will also help improve standards compatibility, explained Markus Willems, Synopsys product manager for system-level solutions.

Rohde & Schwarz will contribute its experience and expertise in the segments of signal generation as well as test and measurement

technology, while Synopsys will add algorithms and verification experience. In both cases, the technology aims at the Physical Layer with its associated modulation issues.

According to Willems, Synopsys has software libraries for algorithm development systems. The companies' SPW and System-Studio products enable engineers to model LTE transmitters as well as Physical Layers. ideal receivers which can be used as a reference for real hardware implementations, Willems explained. With existing receiver models, it is possible to simulate end-to-end communication processes. Both FDD and

The company provides functional models of TD-LTE flavours are covered, Willems said.



The companies will verify the LTE and LTE Advanced libraries against Rohde & Schwarz' LTE signal generators. "Among LTE developers, these generators are regarded as a kind of "Gold Standard", Willem said. In addition, Rohde & Schwarz LTE test equipment will be able to directly read the parameters required for each simulation and verification. "Engineers have to set some 60 to 70 parameters for each test", explained Rohde & Schwarz signal generator product manager Simon Ache. "This is a rather complex process". Automating these settings will offer significant times savings in simulation as well as in debugging, Ache said. In addition, the collaboration reduces the risk

> of discrepancies between simulation and test which frequently triggers time-consuming debugging activities.

The collaboration aims at providing a standard end-to-end solution for LTE and LTE Advanced test and simulation. However, no joint products or product packages (kits) are planned. "Synopsys users do not need to buy Rohde & Schwarz test equipment; they won't be confined to one brand", Willems concluded.

> **RENEWABLE ENERGY**

Chips see 25% surge in solar, wind

By Rick Merritt

THE MARKET FOR SEMICONDUCTORS for

solar and wind energy-generation systems will grow 26.5 percent in 2011, after expanding 25.4 percent in 2010 to reach revenues of \$1.4 billion. That was one conclusion from a new report by market watchers at The Information Network.

The chips are "riding on the coattails of huge increases in alternative energy installs in 2010," said Robert Castellano, president of the firm. "Renewable, alternative energy technologies continue to grab the attention of private industries and world governments," he added.

For example, the global market for photovoltaic inverters more than doubled in 2010, driven by major European markets. The top 10 suppliers of inverter systems and subsystems were European, the report said.

The report looks at a range of alternative energy systems including geothermal, nuclear, fuel cells and other energy storage systems.

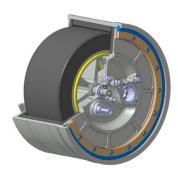
Semiconductors used in these products include MOSFETs, IGBTs, microcontrollers, DSPs, and discrete, it said. ■

Volvo tests flywheel-based KERS

By Christoph Hammerschmidt

IN FORMULA ONE RACING CARS, KERS (Kinetic Energy Recuperation System) help drivers to activate kinetic energy previously stored and thus get the ultimate acceleration in passing maneuvers. Volvo now tests the potential of such a system for volume cars. Unlike most other KERS which store electric energy, the Volvo system makes use of a flywheel.

This autumn, Volvo Car Corporation intends to launch the tests of its flywheel-based KERS on public roads. The system could reduce



fuel consumption by as much as 20 percent and make a fourcylinder engine feel like a six six-cylinder unit, the company said.

The flywheel KERS (Kinetic Energy Recovery System) will be fitted to the rear axle. During retardation, the braking energy causes the flywheel to spin at up to impressing

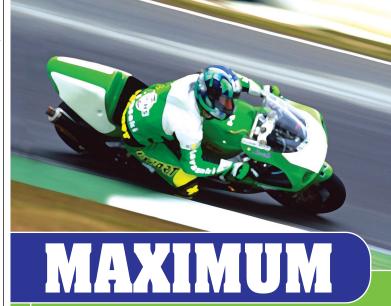
60,000 rpm. When the car starts moving off again, the flywheel's rotation is transferred to the rear wheels via a specially designed transmission.

The combustion engine that drives the front wheels is switched off as soon as the braking begins. The energy in the flywheel can be used to accelerate the vehicle when it is time to move off once again, or to power the vehicle once it reaches cruising speed.

"The flywheel's stored energy is sufficient to power the car for short periods. However, this has a major impact on fuel consumption. Our calculations indicate that the combustion engine will be able to be turned off about half the time when driving according to the official New European Driving Cycle," explained Derek Crabb, Vice President VCC Powertrain Engineering.

Since the flywheel is activated by braking and the duration of the energy storage - that is to say the length of time the flywheel spins - is limited, the technology is at its most effective during driving featuring repeated stops and starts. Thus, similarly to HEVs, the fuel savings will be greatest when driving in busy urban traffic as well as during active driving. If the energy in the flywheel is combined with the combustion engine's full capacity, it will give the car an extra boost of 80 horsepower, and thanks to the swift torque build-up this translates into rapid acceleration, cutting 0 to 100 km/h figures significantly, Volvo engineers have reckoned.

Flywheel propulsion assistance was tested in a Volvo 240 already back in the 1980s, and flywheels made of steel have been evaluated by various manufacturers in recent times. However, since a unit made of steel is large and heavy and has rather limited rotational capacity, this is not considered a viable alternative anymore. Thus, Volvo's flywheel will be of carbon fibre. It weighs about six kilograms and has a diameter of 20 centimetres. The carbon fibre wheel spins in a vacuum to minimize frictional losses.



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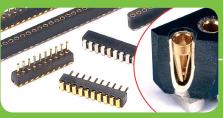
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ASIC prototypes on time - or your money back

By Dylan McGrath

ASIC DESIGN and manufacturing services provider Open-Silicon Inc., claimed an industry first, announcing a money-back guarantee on design engineering schedules.

Under the new program, Open-Silicon will meet a customer's schedule, delivering a prototype on time, or refund the cost of the physical design engineering up to \$500,000, the company said. The offer applies only to designs using process technologies, IP and packaging that Open-Silicon has experience with—designs at 28-nm or using exotic IP or packaging are not covered.

According to Naveed Sherwani, Open-Silicon's president and CEO, the company is offering the program for a limited time because it is confident in its ability to meet schedules and because although customers emphasize the importance of hitting market windows, they often make late changes to a design that cause schedules to slip.

"The main reason we are doing this is because we have learned something in the last eight years," Sherwani said. "The big way to make money is not to argue about the cost of NRE—that's small money compared to what Open-Silicon makes if the product hits the market at the right time. The purpose of this program is to cajole, push, encourage and do whatever is necessary to get our customers' products into the market on time, because they benefit and we benefit."

The "On Time, or On Us," program is set to run through December. Sherwani said Open-Silicon is offering it for a limited time to gauge customer interest. The program covers qualifying designs in 40- or 65-nm process technology. Uner the terms of this program, the originally quoted design non-recurring engineering charge will be refunded, up to \$500,000. for programs that miss the committed development schedule for prototype delivery.

Sherwani said Open-Silicon tracks its on-time delivery rate and reports it internally every month. The company's goal is a predictability rate of 90 percent. Historically, Open-Silicon's predictability rate has varied from as low as 75 percent to a high of about

92 percent, and is currently hovering around 85 percent, he said. In cases when Open-Silicon fails to meet a schedule, the fault rests with customers about 90 percent of the time, according to Sherwani.

"The big debate I'd like to get started in the industry is: why our industry is not as predictable as other industries," Sherwani said. "People say our industry is maturing. In a mature industry, I think it becomes inherently predictable."

Sherwani compared ASIC design to the auto industry. Building a car is just as complicated as designing an ASIC, he said, yet when people go into a dealership and choose the make, model, color and accessories they want in their vehicle, they almost always get it on time. But in ASIC design, schedule slip is often more the rule than the exception, he said.

"It's because there is a commitment." Sherwani said. "I think we should make the commitment as well." Sherwani urged his colleagues in design, test and packaging to create similar programs.

Toshiba to acquire Landis+Gyr

By Julien Happich

TOSHIBA CORPORATION has entered into a definitive sale agreement with the shareholders of Landis+Gyr, under which Toshiba, one of the world's leaders in electronics and power systems, will acquire Landis+Gyr, the global leader in energy management solutions for utilities, for USD 2.3 billion in cash.

The acquisition is designed to create a new growth platform within Toshiba specifically targeting the global Smart Grid opportunity, bringing benefits to both utility customers and consumers. The combination will extend Toshiba's product portfolio and commitment to research and development alongside Landis+Gyr's brand in smart metering solutions. Landis+Gyr has over 8,000 utility customers globally.

Toshiba will retain and enhance the global Landis+Gyr brand. There are no plans for job reduction or restructuring as a result of this transaction.

As of today, Andreas Umbach has assumed the title of Landis+Gyr's Chief Executive Officer and Cameron O'Reilly will become the Executive Deputy Chairman until the closing of the transaction, after which he looks forward to assisting Toshiba in further growing its smart grid business as well as pursuing other private interests.

"Over the past 10 years we have built the world leader in smart metering," said **ENERGY METERING**

Landis+Gyr CEO Andreas Umbach. "As a growth platform for Toshiba, Landis+Gyr will have the resources and power to complement, and indeed accelerate, our product offering to utilities. With this transaction, Toshiba will now share our vision of helping the world manage energy better."

Utility customers will have seamless continuity of operations as well as a broadened product offering to choose from, while Landis+Gyr will gain additional capital strength from being an integral part of the USD 77 billion revenue Toshiba Corporation. The acquisition is expected to close in the third calendar quarter of this year.

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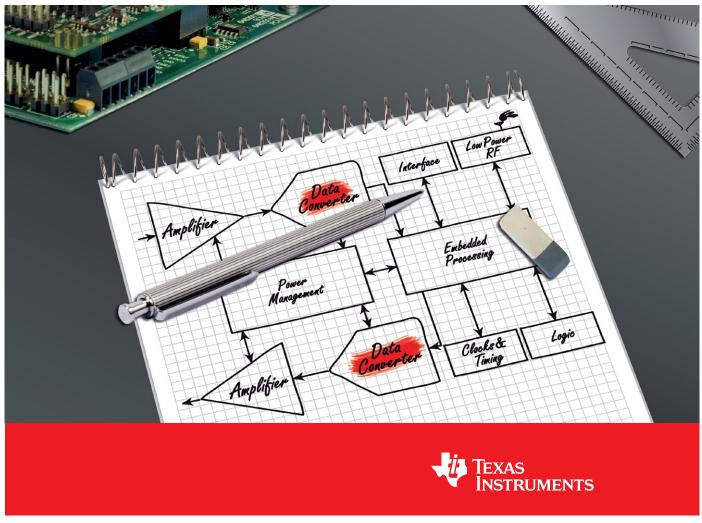
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NXP says it is 'Google Wallet' chip supplier

By Peter Clarke

AS GOOGLE LAUNCHED ITS 'Google Wallet' application for Android smartphones NXP has stressed that it is NXP technology and chips that are enabling the application.

At an event in New York Google, Citi, MasterCard, First Data and Sprint unveiled the mobile payment service Thursday (May 26) saying they plan to roll out the service in the United States over the summer. At commercial launch, Google Wallet will support payments with two payment solutions: a PayPass eligible Citi MasterCard and a virtual Google prepaid card. The first release of Google Wallet is expected to be released on the Nexus S 4G on the Sprint network.

Google relegated its discussion of the hardware behind its wallet to a single sentence saying Google Wallet uses near field communication (NFC) to make secure payments fast and convenient by simply

tapping the phone on any PayPass-enabled terminal at checkout.

NXP put outs its own statement saying it was there in New York at the birth of the electronic wallet. "With NXP's secure contactless NFC solution, consumers can simply wave their phones over intelligent surfaces to pay for goods, apply a discount coupon, or receive loyalty points," the company stated.

It added that its NXP that provides the PN65 component that is the embedded, secure NFC solution for the Google Wallet and that NXP was instrumental in building the application. The PN65 includes the NFC radio controller, the embedded secure element and NFC software in a single device. The secure element provides cryptographic processing to keep mobile transactions secure. The company said its security technology has shipped in over a billion units used in payment and bank cards, access management schemes, mass transit infrastructures, passports, driver's licenses, national ID and health cards.

"NXP's NFC technology essentially converts smart phones into loyalty cards, single-tap location 'check in' devices, concert tickets, coupon carriers, contactless payment devices, transit tickets, and secure keys to access cars, hotel rooms, buildings, and computers -- the possibilities are endless," said Ruediger Stroh, executive vice president and general manager of the identification business unit at NXP, in a statement.

NXP co-founded the NFC Forum in 2004 to help introduce the technology and has had its hardware and software deployed in more than 150 field trials.

Intel Ultrabooks attack tablet market

By Rick Merritt

STILL LACKING A DESIGN WIN in a top tier tablet, Intel is taking another approach pushing down the power and size of notebook computers. Meet the Ultrabook, a slim, low power laptop Intel will describe this week at the Computex trade show in Taiwan

The Ultrabook is a work in progress. Early versions will arrive in cases just 20mm thick and price points under \$1,000 using versions of Intel 32nm Sandy Bridge processor later this year. AsusTek will be among the companies to ship the systems with its UX21 debuting before the end of the year.

"We are very much aligned with Intel's vision of the Ultrabook," Jonney Shih, chairman of Asus will say in scripted comments at an Intel keynote at Computex. "Transforming the PC into an ultra thin, ultra responsive device will change the way people interact with their PC," Shih said.

The Sandy Bridge chips, shipping later this year, will be Intel's first to put an x86

CONSUMER **ELECTRONICS**

and graphics core on the same die, sharing cache memory over a ring bus. Archrival Advanced Micro Devices is sampling similar parts.

Ultrathin, low power laptops running integrated processors have been around for years. Intel aims to push the envelope on the concept with new processors dedicated to

The move comes at a time when leading tablets such as the Apple iPad, Motorola Xoom, Samsung Galaxy Tab and RIM Playbook all have adopted ARM-based chips. Intel launched a new netbook and tablet division last year, but to date it has only garnered a handful of second tier tablet design wins. The Ultrabook concept shows both Intel's frustration at falling behind market trends and gives a gutsy "bring it on" call to leading tablet makers.

Recently, Intel refocused its road map toward mobile systems for both its Core and Atom chips in an effort to catch up. ■

BASF enters Li-ion electrolyte market

By Julien Happich

BASF HAS ANNOUNCED it is entering the business of electrolytes for lithium-ion batteries (LIB) and is forming a global electrolytes team in its Intermediates division. By adding electrolytes to its existing portfolio for the LIB industry, BASF is able to offer another key component for the battery technology.

BASF is already developing specific formulations for high-quality electrolytes based on organic carbonates for customers in the battery and automotive industries. The first products will be commercially available by the end of this year, says the company.

Together with partners in industry and science BASF is developing materials and technologies for today's and next generation lithium-ion batteries. The company is constructing a manufacturing plant for battery materials in Elyria, Ohio/USA. Along with battery materials, plastics and composites for lightweight automotive design and solutions for improved heat management have major roles to play.

SPECIAL FOCUS: EDA & DESIGN TOOLS

Latest emulation innovations accelerate productivity

By Jim Kenney and Kenneth Larsen

AS THE INDUSTRY moves from designing devices with relatively limited functionality to complex, multi-functional and networked devices, traditional techniques such as simulation are coming up short for full-chip verification. This situation is made more urgent as verification continues to increase its share of the total design effort. To keep up, companies need to adopt new virtualization technologies to accelerate verification during chip, system and embedded software development. Ground-breaking moves in this direction include the ability to reuse a single test-bench for simulation and emulation and virtualization of emulation platform peripherals, leveraging the new UVM standard and the potential of co-model channel technology.

A singular test-bench

The Accellera Universal Verification Methodology (UVM) helps verification engineers become more productive in test-bench reuse and test generation. The standardized UVM class library provides building blocks for faster development of well-constructed and reusable verification components and test environments in SystemVerilog. Engineers now have a toolbox that greatly improves productivity.

However, for UVM adopters to be as productive as they need to be, they must overcome the limitations of simulator performance. This can be achieved by enabling the simulation test environment to run on an emulator without modification. Pairing UVM test-benches with co-emulation results in a dramatic speeding-up of test execu-

The ability to reuse a single test-bench for simulation and emulation is a major breakthrough because the RTL for complex or multifunctional designs would slow down a simulator to the degree that it's not practical to simulate. The designs are too deep, the tests take too long. On the other hand, a hardware verification solution will run a test set in minutes that would take a week on a simulator. All the advanced verification techniques can be run on the emulator, including all the features that TLM2 delivers. All these things stay the same on the emulator but run extremely fast.

A single test-bench shrinks the time and effort typically put into creation (because you create it only once), maintenance, and ongoing support for verification environments. And it extends reuse to multiple dimensions because the same test environment can be used on next-generation designs. So companies get the dual benefit of reuse and simulation acceleration. A single test environment

Jim Kenney is the marketing director for Mentor Graphics' Emulation Division. Kenneth Larsen is technical director for Mentor Graphics' Emulation Division - www.mentor.com

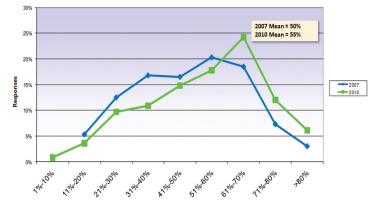


Fig. 1: The percentage of total project time spent in verification has increased from a mean of 50 percent to one of 55 percent. (Wilson Research Group and Mentor Graphics. 2010 Functional Verification Study.)

also produces consistent results because the tests behave the same whether they are on a simulator or an emulator. Using a single testbench helps solve the problem of inconsistent results arising from not testing exactly the same things.

Unleashing emulation

The power and utility of emulation is no longer bound to physical limitations. Until recently all interactions between a design compiled into an emulator and its peripherals was done via hardware devices that represented these peripherals. Functionally there isn't a problem with this but it encumbers design teams with two important limitations stemming from the sheer number of hardware connections required.

First of all, the time and care involved in connecting an intricate and large amount of external hardware to the emulator locks it down to a single project that needs those particular peripherals. If the emulator has some free cycles, another project team would have to disconnect all of the peripherals and cable up their in-circuit emulation solution, and then put it all back together again for the owning project. In reality, that just doesn't happen. So the emulator sits idle while project teams are desperate for emulation cycles but can't get

Secondly, the more physical connections there are, the more things can go wrong. When you start making many connections, reliability goes down. You're going to bend some pins, have some bad cables, bad connectors, loose connections, and so on. And if something fails, finding the cause is like trying to untangle a Gordian knot.

A promising solution is to virtualize the peripherals. Virtualization takes the hardware out of peripheral representations. Instead, part of the peripheral is modelled in the emulator and part of it is modelled as an application in a workstation, using co-modelling channels and transactors instead of physical cables and equipment.

The entire environment, both the design inside the emulator and the devices needed to exercise the peripheral interfaces, is a virtualization and can be software configured. The emulator becomes a flexible, general purpose resource, where any project team can schedule or grab free time on the emulator. They can virtually configure the emulation instantaneously, run their jobs, and then the next group can reconfigure it to suit their design.

Already multimedia and video, Ethernet, PCI Express, and SATA controllers can be done virtually and are very easy to configure. Emulation solution vendors will keep broadening this portfolio to other disk drive protocols like SAS and any other peripheral that you can imagine. Virtualizing the peripherals increases the emulator usage. Designers don't have to go into the lab and physically reconfigure it with external hardware solutions. It can be reconfigured with these virtual solutions by software from any location on the planet and more people get access to the advantages of emulation in terms of performance, capacity, system-level design and verification and so on.

Co-model channel

Emulation has always been about performance and capacity, faster than simulation, big enough for the largest design and it still is. But the technology is evolving beyond these two fundamentals in terms of all what you can do virtually that used to require a physical hardware connection.

Driving this paradigm shift is the co-model channel technology that underlies virtualization and enables simulation acceleration, software execution debug and virtual peripherals. Co-model channel technology was developed to accelerate transaction-level test-benches, rocketing stimulus data from a workstation to transactors in an emulator over the co-model channels. Virtual peripherals use this same transport mechanism to stimulate a design.

How much faster is emulation? Bypass marketing claims and simply calculate it yourself. Assume the emulator will run your design at 1 MHz, plus or minus a few hundred KHz. This is the frequency of the fastest clock in your design. Now determine how many times that clock toggles each second of wall-clock time during simulation. If your simulation can run 100 clocks/sec, the emulator will run 10,000 times faster. This is the best possible throughput and must be de-rated to account for test-bench overhead. With a well written test-bench it's not uncommon to see de-rating factors of 20%, resulting in an acceleration factor of 8,000X. If your test-bench performs a lot of calculations for each test vector sent to the design, the de-rating factor will be worse.

Accelerated transactors run in the emulator and expand a transaction from the test-bench into pin-level stimulus. A well written accelerated transactor can run at full emulation speed (1 MHz) and have a typical expansion factor of about 10X for a simple protocol. To keep the emulator fed and running at full speed your test-bench must produce transactions at a 100 KHz rate. Anything slower will cause the emulator to wait, resulting in the de-rating factor mentioned above. There is a wide range in expansion factors, depending on the complexity of the interface protocol. Ethernet for example will expand a packet

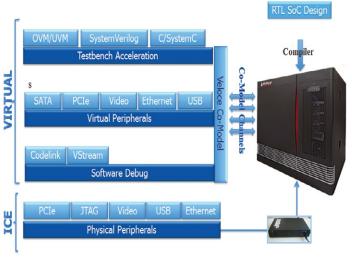


Fig. 2: Co-model channel based virtual solutions offer three powerful emulation solutions: simulation acceleration, software execution debug, and virtual peripherals.

(single transaction) into hundreds or thousands of emulation clock cycles depending on the frame. Emulation can run what would be a two week simulation in just five minutes.

Software execution debug tools can also be connected to an emulator via transactors and co-model channels, allowing you to stream information out of the emulator that will drive off-line software debug. You don't need a hardware probe for every type of processor you're using. You use a co-model channel and the virtual capability to do the same type of debug you did before via JTAG. And it's completely reconfigurable. This supports a lot more software engineers with the same amount of hardware.

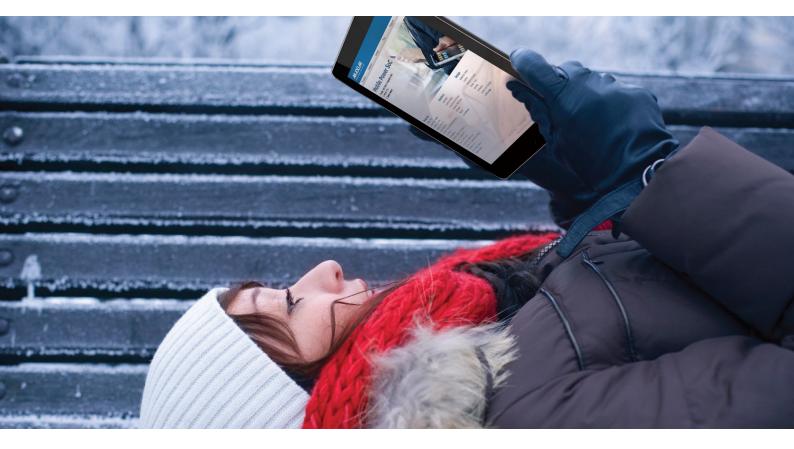
Customers have been concerned about how many IO pins were on the emulator. Emulation architecture will increasingly focus on improving co-model channel throughput because more activity is passing through the co-model channels. As emulators get faster and more applications are applied in parallel, the co-model channels won't be the limiting factor.

All of this is going to change the way people work in the future. It's going to broaden the application of emulation because a lot of companies that could benefit from emulation have until now been deterred by all of the external hardware and the lack of a flexible usage model. With co-modelling and virtualization the emulator becomes an emulation cabinet with a rack full of workstations all completely software configurable, easy to set up, and quickly reconfigured to connect different peripherals and different software debugging technologies through a GUI. This is a very familiar configuration that will make it comfortable for engineering teams to benefit from the full power of emulation, which until now has been under-exploited.

A hardware verification computing solution that offers virtualization, co-model channel technology and a single, reusable UVM testbench for simulation and emulation will ease the path to wider adoption of emulation and increase its value for designs with blocks above 10M gates and very long test sequences such as video, networking, signal processing and codecs. Leading semiconductor and electronics systems companies already embrace to an extent the technical and economic benefits of emulation. Five years from now people will still be simulating but they will not be simulating large systems. These are going to be verified using hardware emulation. The goal is much faster end-to-end verification of the entire development process.

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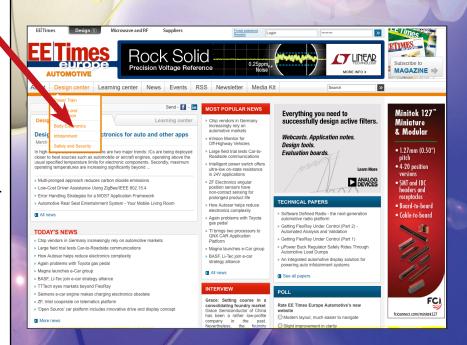
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Cloud-based verification could prove to be disruptive 300

TODAY WE LIVE in a world of constant change. This is the essence of the free market and while this trend assures that consumers have something new to buy, it makes the engineers' jobs ever more difficult. Competition today continues to drive growing design complexity from generation to generation, while simultaneously reducing the verification window. For engineers, this translates into a worst-case scenario: exponentially growing verification complexity and shrinking schedules. For the IT/CAD manager, this translates into unsustainable demand for additional verification compute resources, just as they're trying to reduce costs.

It is no wonder that companies today are looking for a paradigm shift in verification methodology, something that will fundamentally change the equation. That change may be cloud-based verification computing. Since this represents a fundamental change in thinking, it drives us to understand and learn how to overcome the challenges, real and perceived, that a cloud environment introduces to verification, along with the unique benefits that cloud computing brings.

One of the fundamental benefits of cloud-based verification is its ability to scale resource availability dynamically to meet verification demand variability. Verification compute resource demands tend to peak and wane throughout the project. Early in the design cycle, engineers are focused primarily on block-level debug. The bug rate is high and development progress is limited by the number of verification engineers. As the design becomes more mature and verification moves to full system level simulation regressions, bug rates fall (as does simulation speed). Progress is limited by available verification compute resources.

This scenario creates special challenges for CAD and IT managers. When verification compute resources are combined across multiple teams, these variations can align - cre-

Lawrence A. Vivolo is director, solutions marketing at Synopsys - www.synopsys.com he can be reached on lvivolo@synopsys.com

ating large swings in demand - see figure 1. Historically, these peaks and valleys have been addressed by either over-provisioning compute resources (buy for the peak) or under-provisioning resources (ignore the peak and extend schedule). This is precisely the type of application that is ideally suited for cloud computing.

Cloud-based verification provides the scalability to access hundreds of simulation servers rapidly as well as the ability to turn off the servers (and stop paying for them) once they're no longer needed. This provides several economic benefits. In addition to avoiding schedule delays, having virtually infinite resources means that engineers can compress schedules. If a week-long regression could be completed in a day, early market entry would be possible, leading to more revenue and higher market share - see figure 2. Cloud computing also requires no additional CAPEX because it is an operating expense (OPEX). CAD managers may then have the flexibility to spend more money on other needed resources.

There is no question that cloud-based verification computing can provide a costeffective alternative to large investments in verification compute-hardware. But there are some methodology considerations that should be understood prior to adding cloudbased verification to your existing verification infrastructure.

For example, most providers offer an application programmer's interface (API) for configuring, creating, managing and destroying clusters within the cloud. Verification engineers will not want to deal with this low level interface. Developing an easy-to-use interface is complex and could delay cloud deployment. To avoid this, Synopsys provides intuitive, GUI-based interfaces along

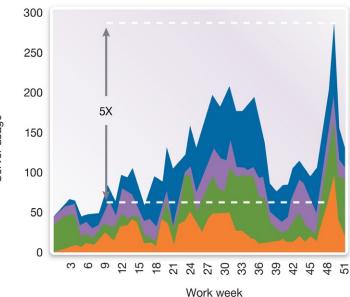


Fig. 1: Large demand variations impact compute resources

with a Unix-based command-line interface that enable customers to immediately leverage the cloud.

The next area of consideration is performance. Many cloud providers are leveraging existing server hardware and infrastructure for cloud - which was typically architected for client-server applications. Simulation, on the other hand, generally uses the most powerful computers available, each with plenty of memory. Beyond the server itself, simulation performance can be impacted by how the server cluster is architected. How much local scratch memory is available for each core? How is each server connected to storage? With simulation regressions, you'll want to move the design image to a centralised disk accessible by all the servers within the cluster. This is great for simplicity and cost, but requires a high performance network and storage array. Synopsys recommends cloud providers with high-performance, multi-core servers using 10GbE minimum connectivity to/from network-attached storage (NAS).

Verification coverage is also impacted by storage architecture. With coverage, each individual simulation can generate large coverage databases. Storing this data on the centralised storage array would degrade shared disk access. A better solution is to architect this traffic to leverage each server's on-board scratch disk.

Network performance between your local data centre (ground) environment and the

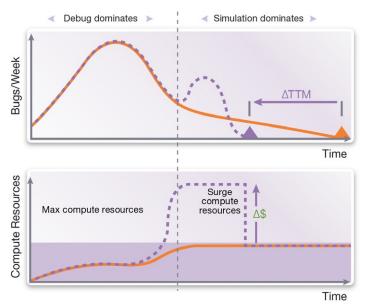


Fig. 2: By adding large quantities of surge compute resources, time to market can be greatly reduced.

cloud should also be considered. To maximise network bandwidth, traditionally chatty applications (such as interactive debug) should use thin-client protocols. Even better, deploy a methodology where debug is completed on your local servers. Likewise, transfers of large amounts of data should be made only when necessary. (Fortunately, the design image itself is typically only transferred to the cloud once). For coverage data, for example, Synopsys recommends that the individual coverage databases are merged on the cloud, leaving only the final results to transfer.

Virtualization is another area that should be reviewed when adding cloud to your verification environment. Hard-coded paths to disk drives should be avoided in a virtualised cloud environment since these drives will not be available on the cloud. Instead, use relative paths or environment variables to specify such paths. The same can be said for other centralized resources, such as 3rd-party license servers, EDA tool paths, etc.

Finally, engineers should remember that the cloud introduces several new business models. As such, some areas to be aware of include security; cloud computing providers are likely more secure than the average enterprise. Synopsys-approved cloud providers undergo independent security audits regularly, and have industry-accepted certifications such as ISO27001/27002, SAS 70 Type II and others.

Corporate policies should also be considered; many companies have policies on moving corporate IP offsite. These policies typically must be reviewed, and should be updated as needed.

Automation is another area that needs evaluation; extending a verification environment to the cloud can be straightforward, depending on the customers' requirements. Synopsys recommends working with an experienced partner to make the initial transition faster.

With its ability to dynamically grow and shrink resource availability to meet changing demand, coupled with financial benefits like pay-as-you-go computing, cloud-based verification represent the next paradigm shift in verification methodology. When mated with existing infrastructure, it delivers dramatic increases in verification throughput while simultaneously optimising long-term costs. With the right EDA partner, a carefully selected cloud provider, and a little planning, cloud-based verification can be introduced with minimal challenges.

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Bringing the invisible to the engineers' eye with near-field scanning

By Thomas Mager

THE ADAGE "A picture paints a thousand words" results from the fact that we experience a major part of our perceptions with our eyes. Electromagnetic radiation is always surrounding us.

However, the visible wavelength reaching our eyes is only a small fraction of the entire spectrum, leaving the major part of the wavelengths interesting for technical applications invisible to the human eye. As the demand for communication-channels is constantly rising, the electromagnetic spectrum becomes a precious good that must be optimized and the amount of electromagnetic energy present in the vicinity of electronic devices is increasing. On the other hand, miniaturized structures and supply voltage reductions in digital and mixed signal systems result in high requirements on the electromagnetic compatibility (EMC). Therefore, in order to design reliable systems, today's engineers have to be aware of the generated as well as the surrounding electromagnetic fields.

Visualizing electromagnetic fields

A well-known technique to visualize electromagnetic fields can be found in the area of near field antenna measurements. Visualizing the near field distribution gives designers an intuitive way to pinpoint the location of a malfunction like a broken connection in the feeding network of an antenna array. The field distribution can be mapped using a near field probe like an open ended rectangular waveguide positioned at various locations in front of the antenna. The measured output signal at the waveguides terminal detected at various locations in front of the antenna can be used as an input for a subsequent data processing, finally providing information like the field distribution or the antenna pattern.

Another approach to look at a system's electromagnetic behaviour is to carry out numerical field simulations and analyse the computed field distribution. These techniques are successfully employed in a wide range of applications if the analysed system is well defined by considering material parameters, exact geometry definition, access to an adequate model of all the analogue and digital as well as all the linear and non-linear parts of the system. Typically for a complex electronic system, the available information is not complete. Additional effects such as aging and manufacturing tolerances prevent a purely simulation-based evaluation of hardware modules. The dynamic range to be taken into account (for example the biggest dimension may be the length of a heat sink and the smallest parameter might be the radius of a bond wire) further complicates numerical field calculations. There currently is no unified simulation platform allowing for the intuitive analysis of the global system with its hybrid components.

Often, an understanding of parasitic EM phenomena is needed in the final design stage. While a modular demonstrator with well

Thomas Mager is deputy head of department/ group leader at Fraunhofer ENAS - www.enas.fraunhofer.de/EN/abteilungen/ase/ -He can be reached at thomas.mager@enas-pb.fraunhofer.de

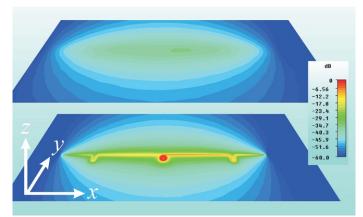


Fig. 1: Simulated magnetic field strength above an RFID-tag-antenna. The field distribution shows more details with a higher amplitude when evaluated near the antennas surface.

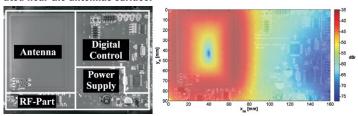


Fig. 2: An RFID-reader consisting of different functional blocks (left) and the magnetic field distribution measured at the Fraunhofer ENAS at the operating frequency at 13.56 MHz (right).

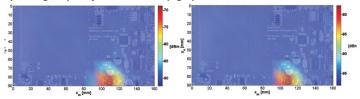


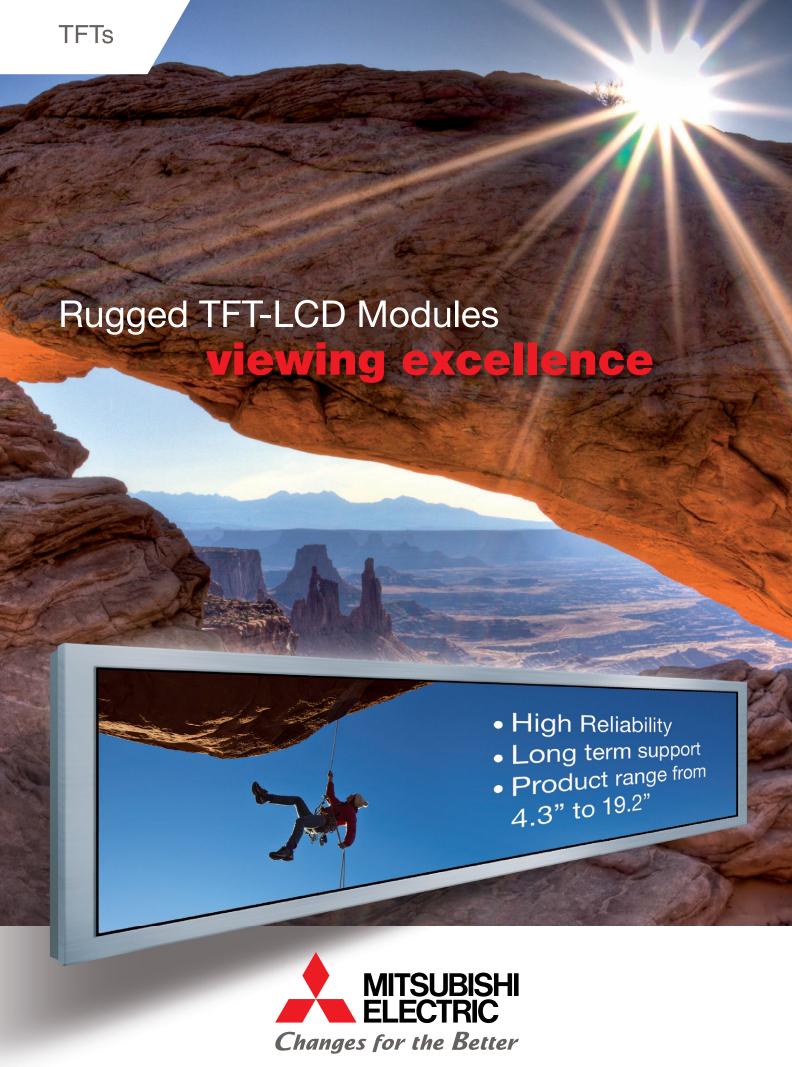
Fig. 3: The measured magnetic field distribution above the reader at 157 kHz (left) which is the operating frequency of the DC-DC converter and its first harmonic at 313 kHz (right).

separated functional elements might perform well, the EM reality might become different if all elements are brought together in a fully integrated prototype. When a product release date is fast approaching, design modifications to remedy unwanted EM effects might be applied on the basis of suspected EM-couplings lacking well-considered justifications. This is when an EMC near field scanning system will bring extra visibility.

Pin-pointing electromagnetic emissions

In a case study, Fraunhofer ENAS had to investigate an integrated RFID interrogator whose reader antenna operating in the HF-band was implemented on the same PCB as the power management electronics and the digital part controlling the RF-transceiver circuit and the external communication bus infrastructure.

Tested as a modular system, the design was exhibiting a good



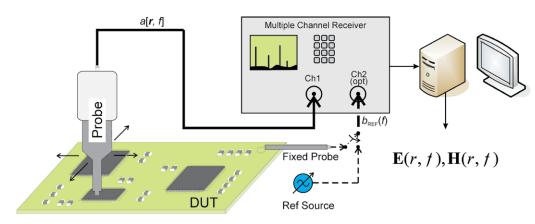


Fig. 4: Conceptual representation of a near field measurement system.

performance. However after the integration of all of its parts on a single PCB, the system suffered from a poor read range. Because the on-board antenna generated a strong magnetic field, one could suppose that a parasitic inductive coupling at the fundamental frequency of the RF part was harming the integrity of the logic levels on the digital control bus.

Though, a fist scan could clearly show the absence of a localized hot spot in the magnetic near field at this frequency. Extending the frequency band from a few kHz up to the MHz region revealed a localized magnetic emission originated in the power supply section. A choke at the output of a DC-DC converter was clearly identified as being the source of the emissions, which coupled to the RFID antenna overlaying to the weak modulation sidebands of the RFID uplink. The performance was significantly enhanced after modifying the DC-DC converter so the whole system could meet the wanted specifications.

Designing an EMC near field scanning system

An EMC near field scanning system is composed of a near field mapping probe, a mechanical probe positioning system, a measurement receiver detecting the signal picked up by the probe and an optional reference probe positioned in a fixed location with respect to the device under test (DUT) allowing for the evaluation of the phase of a

Metal free portal Inlay for DUT-Mounting Ground Plane-Granite body ducing vibration

Fig. 5: Mechanical components of an advanced near field scanner NFS 3000 as it is available at the Fraunhofer ENAS.

free running DUT.

The near field mapping probe is designed for localized coupling of a dedicated field component to the DUT emissions over a broad frequency range. The mechanical precision of the probe positioning system is a crucial factor determining the accuracy of the measurement results. While antenna nearfield measurements are typically carried out at a relatively long distance from the device under test, investigations regarding the EMC of electronic systems have to be carried out at a very close range. The mechanical drive system should allow for a smooth motion of the probe to prevent mechanical vibrations of the probe's tip. One way to minimize probe vibrations is to move the DUT instead of the probe.

This is the approach that Fraunhofer ENAS and the University of Paderborn implemented in the NFS 3000 System developed by Magh & Boppert - www.nfs3000.com. Such a setup also lowers stability constraints

on the probe mounting system, allowing the use of lighter non-metallic materials which also reduce the field distribution distortions caused by the scanner body.

The measurement time required for a near-field scan is determined by the measurement receiver. While frequency swept receivers with a narrow resolution bandwidth provide the high dynamic ranges necessary for the huge differences in emissions in the area of

EMC, time domain approaches provide outstanding measurement speed.

In order to combine the benefits from both approaches, a vector signal analyser can be used to measure a fraction of the spectrum in the time domain with a high degree of quantization which results in an acceptable dynamic range. The electrical behaviour of the DUT might cause unpredictable sudden



Fig. 6: A set of near field probes designed for various field components.

emission for instance due to a major malfunction. In this case the components of the signal acquisition chain have to be protected.

This can be done by permanently monitoring the probes signal power over a broad frequency range in combination with a signal interruption like a coaxial relay. This protective device can be combined with a low noise amplifier and adjustable attenuators extending the probes signal input range for a huge variety of applications.

Together with the NFS 3000 near field scanner, specific controlsoftware is necessary, the usability of which is critical. Dedicated control software developed by Magh & Boppert prevents the setup of erroneous parameters so as to avoid the collision of the probe tip with the DUT even when it follows the profile of a complex circuit design at a few micrometres above the surface during a measurement.

The huge amount of measurement data accumulated during a scan has to be handled efficiently and presented to the user in a meaningful way too. Near-field EMC scanners can be used in an intuitive way to identify parasitic coupling in electronic components, reducing evaluation periods and allowing for targeted design modifications to enhance product reliability.

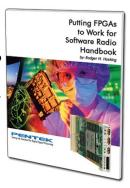


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Cloud-based development moves one step closer

By Philip Ling

THE CONCEPT OF CLOUD-BASED development is beginning to entice EDA companies; it not only offers a simpler distribution mechanism for what can be very large installation packages, but could present a number of new business models, particularly in the management and distribution of design files.

There may never be a 'good time' to make the switch away from locally hosted tools, but finding a design environment that offers all the tools an engineering team requires would, presumably, be the first step towards a cloud-based collaborative development paradigm and it is one that Altium hopes to attain with the latest version of its development environment, Altium Designer 10.

It attempts to bring together all of the elements necessary for embedded development in to a single environment that can be licensed across an entire engineering team and, with the latest version, manage that development from a central repository of design files that can be checked in and out, version-controlled and passed for production.

For some this may represent the ultimate development paradigm; where design files are not only automatically backed up, but allow multiple engineers to develop parts of the same design in isolation without fear of ever working on an out-of-date version.

Fundamentally, Altium Designer started life as a PCB design tool and it retains this feature, however since its inception in the mid 8os, it has been developed to incorporate architectural features that now provide the framework for a cloudaware environment, as well as extending its design features to include CAD, FPGA and embedded software development. The result is AD10 which, in both theory

and practice, offers the ability to move from concept to finished product in a single, or unified, design environment. With the latest version much of this is now managed in the 'cloud', albeit only in theory at the moment.

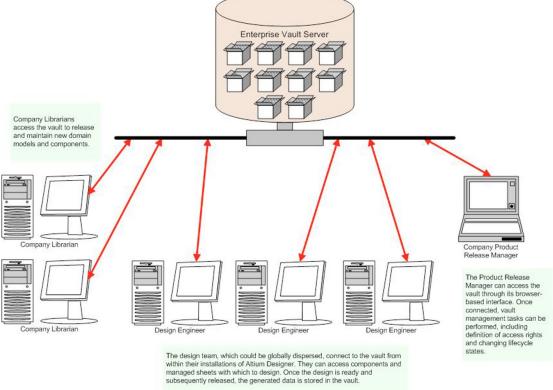
The unified concept forms a large part of Altium Designer's unique strength, but it may also spell disappointment for some engineers who will undoubtedly have their own preferred tool suite for some development stages. And this really is the fundamental buy-in needed to adopt AD10; the idea that it can and should be used for all major parts of embedded development.

This is something akin to the large following that National Instruments enjoys with its graphical design language, LabView. A design tool like LabView, or AD10, can polarise developers; those that absolutely love it, and those that don't. Unfortunately, there really doesn't seem to be a lot of middle ground with AD10, as many of its major benefits come from using it as intended,

as a unified environment across multiple disciplines.

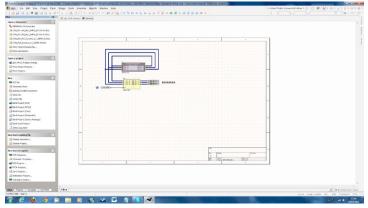
Models at different levels of abstraction enables other members of a corporation not directly involved with product development to access vital data, through Altium Live - which is essentially a browser based portal. This, along with the concept of Vaults, allows data files to be accessed remotely to alter their status, checked in or out of the repository or simply viewed for reference. That may be the goal but, today, it remains just out of reach, as some features of AD10, including the vaults, are still in need of

As a development environment, the complexity of AD10 may also be apparent to users, which isn't necessarily a good thing. Context-sensitive menus make it sometimes difficult to navigate, while the sheer capability of the environment means it's often difficult to know exactly which menu or tabbed screen you need to be working on.



The Vault concept makes design files available to the entire development team.

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Alitum Designer 10 is a unified development environment which provides a single platform for PCB, FPGA and embedded software.

and access design files.

Being able to globally versioncontrol components, and distribute them

via a secure vault will undoubtedly present massive productivity gains for many developers. Moving to a unified development environment will likely appeal to a great many OEMs; it simplifies so many aspects of development, even if it does impose some restrictions. For many, and as AD10 continues to evolve, those restrictions will be less important than the (potential) productivity gains it offers.

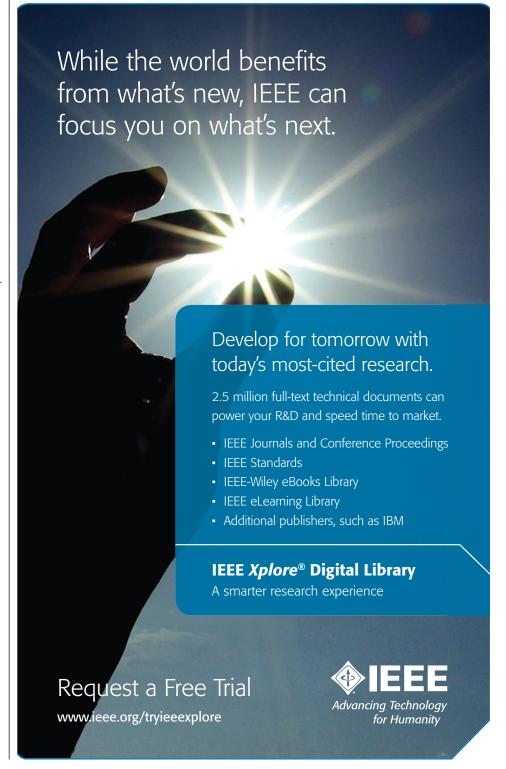
This is an observation based on limited time to become familiar with the environment. but it does illustrate that new users to AD10 will need to spend some time on the steep part of a learning curve before real development can begin.

The unified environment isn't limited to the PC screen; AD10 is complemented by physical development platforms, called Nanoboards, that can, again theoretically, be used instead of board support packages and home-spun prototype boards. The unified environment itself is project based and well integrated, so that a new design requires a new project, which is then expanded in the project view to reveal all of the design files used in the project.

While the project-based approach is structured, some engineers may find it too rigid and even though one of the fundamental concepts behind AD10 is creating portable designs using generic FPGA (VHDL/Verilog) components, it can require the use of devicespecific libraries when using an FPGA with specific features. This library, in turn, must be imported to the project before it can be

The wide-ranging capability of AD10 does raise the question about engineering disciplines, insomuch as engineering teams normally include a PCB designer, FPGA developer and embedded software specialist, but how often are they the same engineer? It follows that, if they aren't, then the whole engineering team needs to standardise on a single environment - giving new meaning to the word 'unified'.

With vaults - Altium's preferred name for databases that may be stored locally, on an intranet or in the cloud - design file sharing becomes more feasible. At the moment, while users can access two of Altium's vaults through AD10, the cloud-based user-defined vault service is still in beta, but the concept is valid and it follows that when it is production-ready, many of Altium's customers will benefit from using the cloud to store, share



Bio-inspired robots dig into nature's evolutionary designs

By Julien Happich

THE INTERNATIONAL WORKSHOP on bioinspired robots which took place at the Ecole des Mines de Nantes, France, last April was an opportunity for many researchers to showcase their latest prototypes of crawling, swimming or flying robots, all trying to mimic some of wild life's most elegant and energy-efficient locomotion solutions. The workshop was coorganised in the framework of the European projects ANGELS (ANGuilliform robot with ELectric Sense) and LAMPETRA (Life-like Artefacts for Motor-Postural Experiments and development of new control Technologies inspired by Rapid Animal locomotion) as well as by CNRS (Centre National de la Recherche Scientifique).

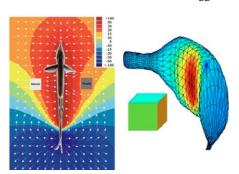
Frédéric Boyer, professor at the Ecole des Mines de Nantes and one of the hosts of this workshop, is very talkative about nature's clever evolutionary designs and his fascination for the animal kingdom is shared among many robot designers. "Finding design inspiration in nature is not something new", he explains, "the Shinkansen Japanese bullet train's nose was directly inspired from the kingfisher's beak. The bird's capability to dive and hit the water surface at high speed gave designers the necessary hints to reduce the shockwaves that the high-speed train experienced when entering the many tunnels of the mountainous Japanese landscape". "Another great example of locomotion could be taken from the shovelsnouted lizard of Namibia, capable of navigating through sand with apparent ease. There may be a case of supra-friction boundary phenomena occurring between the Lizard's scales and the fine grains of sand. Studying this could certainly yield new ways to design inspection robots capable of moving in 3D through grain storage silos for example." Boyer says.

While the last 20 years in robotics have been spent designing mostly wheel-based platforms with enough embedded computing power to crunch sensors' data into various obstacle recognition and avoidance strategies, the branch of bio-robotics seeks to couple locomotive action directly with sensory feedback. The idea is to couple basic modules of action/ perception and embody intelligence into the robots' morphology for optimum locomotion

even in unknown environments. Rather than trying to bring everything back to an analytical problem or trying to solve compute-intensive equations, this approach aims at finding stable and self-guided locomotion scenarios that do not rely on a centralized brain or on landscape interpretation. Artificial intelligence would only be needed for high-level decision-making, not for basic locomotion or sensory tasks.

Coordinator of the ANGELS project - www. theangelsproject.eu, Boyer gives us an interesting analogy. "You don't need to measure precisely a doorway, or even name it or identify it as being rectangular or tubular in order to cross from one room to another. Yet this is what most vision-equipped robots do when relying on image processing. In the ANGELS project, we are trying to emulate certain fishes' electro-sensing capabilities that enable them to "feel" obstacles at close range in order to navigate through murky waters".

Some fishes like the Gnathonemus petersii are capable of polarizing isolated sections of their body at different electrical potentials, forming a bubble-shaped electric field. Any object found within the electrical field will affect the electric current passing across the fish's electric sensors and can be perceived as an electric image - see fig 1. In effect, the electric field acts as a proximity-sensing skin performing some type of remote haptics, at about the distance of the robot's total length. The ANGELS project's aim is to design small individual propeller-driven modules or "agents" capable of communicating with each other and able to self-assemble into a bigger



The electro-sensing capability of Gnathonemus petersii enables the fish to perceived objects as an electric image.



The lamprey/salamander bio-inspired LAMPETRA making some waves.

eel-like robot for undulatory swimming. Having reached a specific area of interest, the small agents could split to perform detection tasks in a swarm mode, and assemble again for better swimming efficiency during long distance navigation when inspecting industrial conduits for example. The first modules were demonstrated in a small pool during the workshop, exhibiting small propellers for 3D locomotion before magnetic coupling. After docking, the connection system used a screw mechanical connection to transmit the forces required for swimming from one module to another. Studding each agent with up to 16 receiving electrodes, future research will look at synchronizing the module's position (in the eel-like swimming assembly) with the data acquisition to test various electro-sensing algorithms in real time. Another project under development at the Ecole des Mines de Nantes is the 2.7m long Robot Anguille Autonome en Milieux Opaques (RAAMO or autonomous eel robot in opaque media), featuring 123 vertebrae for hyper-manoeuvrability in confined environments.

Other kin swimmers demonstrated their ease in the crystalline water, like the lamprey/salamander bio-inspired LAMPETRA developed at the university Scuola Superiore Sant'Anna, in Italy. Combined with advanced numerical simulations, the salamander lookalike robot - www.lampetra.org - is used to study goal-directed locomotion by mimicking the neuronal connection, the biomechanical structure and the control functions of salamanders. Bio-inspired robotics involves many specialists from life sciences, including neurobiologists. Such cross-domain collaboration has enabled roboticists and neurobiologists to understand the function of the lamprey's spinal cord and translate it into command algorithms for swimming robots.

Again, the whole idea is to cut processing

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power short and build a reactive sensory system that does interact in real-time through the integration of a neural system capable of linking directly perception to action and the perception of action.

Flying robots were also present at the workshop, with Dr Hao LIU from Chiba University, Japan, presenting some of its Micro Air Vehicles (MAVs) robots capable of stationary flight among other flapping wing drones such as the DelFly Micro, weighing 3.07g with

a 10cm wing span, from the Delft University of Technology, Netherlands. The DelFly features an on-board camera used to extract optic flow information for obstacle avoidance in autonomous flight. The algorithms running behind the pixels is directly inspired from fly vision



The MAVs robots capable of stationary flight.

where luminosity variations and flow optics at pixel level rather than full images provide cues for stability and collision avoidance.

Soft-bodied robots form another exploratory branch of bio-inspired robotics, moving away from rigid articulated constructions to soft elastomeric compounds combined with tendon-like cabling or shape memory alloys (SMAs) that mimic muscle actuation.

The Octopus project - www.octopus-project. eu - is aimed at replicating the octopus' amazing dexterity for use in marine applications such as cleaning, exploration, monitoring, maintenance and rescue. This brings up the concept of continuous soft robots (CSRobots) made of elastic elements with ideally infinite degrees of freedom, a special class of hyperredundant robots where the number of short rigid links is high. Federico Renda, researcher at the Research Centre on Sea Technologies and Marine Robotics from Livorno, Italy, explains: "so far, we have built one octopus-



This manipulator arm directly inspired from the octopus' tentacles boasts infinite degrees of freedom. Source photographer "Massimo Brega - The Lighthouse".

like robotic arm prototype, made up of soft components only, including silicone and embedded cables laying conically around the main

The next stage is to integrate eight arms into a single unit and develop a control algorithm for the coordination of those arms. Then we may be able to tune it for specific applications". Renda describes the grip strength of the arm as being proportional to the difference between the

"natural" curvature of the robotic arm and the curvature of the object being grabbed. The arm is also equipped with passive suckers. The poster on display also gave some details about the radial arrangement of transverse actuators as a mechanism for up to 23% of diameter reduction to enhance arm elongation up to 70% (the arm being a constant volume structure with a variable length to width ratio). Even the sinusoidal arm nerve in the real octopus gave the researchers some hints towards the use of stretchable electronics arranged into wavy

Caterpillars offer other interesting models for roboticists trying to build all-terrain capable soft-robots that can adjust their shape to whatever obstacle. In a paper yet to be published, researcher Orki Omer from the School of Mechanical Engineering at the Faculty of Engineering of Tel Aviv University presents his team's project of a robot composed of struts and cables that could mimic caterpillar locomotion. The cables are to emulate the longitudinal muscles while the strut would stand up for a caterpillar's proleg as part of a hydrostatic skeleton. The researcher explains that using what they call Assur Tensegrity elements, or deformable but highly stable structures featuring tensional integrity, they are able to model complex movements while ensuring a high degree of fault-tolerances in locomotion.

Researchers from Tufts University, Massachusetts, have been prototyping soft-robots for a number of years based on the Manduca sexta caterpillar also known as the tobacco hornworm. Director of the Biomimetic Devices Laboratory created in 2005, professor Barry Trimmer has come up with various silicone-based prototypes of different lengths (up to half a meter long and 5cm in diameter). Featuring embedded SMA coil actuators

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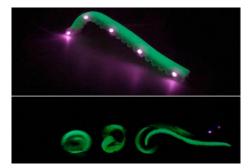
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The caterpillar soft-robot from the Tufts **Biomimetic Devices Laboratory is capable of** crawling but can also jump into ballistic rolling.

controlled by electric pulses, the prototypes are capable not only of crawling, but can also be set into ballistic rolling, an emergency trick used by some caterpillars and salamanders to quickly propel themselves away from predators. Professor Trimmer and his team have just designed a 10cm long soft-bodied robot, called GoQBot, to replicate the functional morphologies of a caterpillar. "It is the non-linearity of the mechanics that makes soft-robot modelling such a difficult task for our mathematicians" explains Trimmer whose background is in neurobiology, "the control elements remain the same as in earlier prototypes but better modelling and mechanical coordination of the actuators was required for GoQBot to thrust itself off the ground into a ballistic roll in less than 100ms, at over half a meter per second". The lab is also investigating passive grips with retractable pads (active release only) that would enable the caterpillar to hang firmly to thin vertical obstacles for hours while still being energy efficient.

Soft robots can be built with flexible and resistant polymer materials that are well suited for marine environments. Hydrostatic deformable constructions allow roboticists to modulate the shape and movement of their creatures by continuous flexure, rather than by segments, which is a definite advantage for all sorts of gliding and swimming robots.

The Aqua ray marine robot designed by Festo AG & Co. KG came from the observation and analysis of manta rays' submarine "flight" and gliding expertise. The slow flapping motion of the ray's fins combine maximum propulsion with minimum energy consumption. The Aqua ray features a water-hydraulic drive unit and Festo's fluidic muscles consisting mainly of hollow elastomer tubes with integrated woven aramide fibres, wrapped in a 3D-deformable skin. Filled with air or water, the fluidic muscle's diameter increases and the actuator contracts longitudinally in a smooth flowing elastic movement. This combines with a so-called Fin Ray Effect coming from the non-linear response of the fins' structure under flexion. The 61cm long robot, with a wing's

span of 96cm, can be operated either as a very energy-efficient hydrostatic glider or with actively flapping wings. The manufacturer sees it fit for the inspection of pipelines, cables or the sea floor itself. The German company also designed the AquaJelly, an artificial autonomous jellyfish capable of communicating with other AquaJellies in order to adapt its swimming pattern and emulate a swarming behaviour. Each AquaJelly consists of a translucent hemisphere hosting a central watertight body and eight tentacles for propulsion in a wavelike motion, using the Fin Ray Effect. The central dome houses all the electronics, including pressure, light and radio sensors, white and blue LEDs and eleven IR LEDs which enable pulsed infrared optical underwater communication between several AquaJellies. Two concentric conductive silver rings on the outside allow the AquaJelly to connect its charging control unit to charging stations located above the water surface. ZigBee is used for surface communication with the charging stations and to signal to other AquaJellies at the surface that the station is occupied. The pressure sensor allows the AquaJelly to control its depth of immersion to within a few millimetres and a four-armed pendulum controls the robots' centre of mass, determining its inclination and thus its spatial direction. Their reported swimming autonomy is 8 hours before recharging.

Also borrowed from nature, swarm behaviour is opening up a new branch of robotics where large numbers of small robot modules are expected to offer more resilience and more adaptability than a single expensive robot dedicated to one task. In the case of the AquaJellies, a swarming pattern emerges from a basic set of rules defined by the necessity to avoid collision while staying within communication reach, re-charge efficiently by swimming strategically in the right direction (depending on which stations are free) and maybe other conditions that will optimise the task for



The AquaJelly's LEDs and light sensors enable the robot to communicate with others and emulate a swarming behaviour.

which the AquaJellies have been programmed. The whole challenge of swarm robotics, apart from the modular design of self-assembling multi-agent robots which in itself is nothing trivial, is to define the simple rules from which a collective behaviour pattern will emerge and maximize the efficiency of the whole multirobot system.

Several European Commission funded research projects are in place that focus on swarm optimisation, including the REPLICA-TOR project (Robotic Evolutionary Self-Programming and Self-Assembling Organisms) - www.replicators.eu - and the SYMBRION project (Symbiotic Evolutionary Robot Organisms), both started early 2008 and due to run until 2013. Investigating new control models for robotic systems consisting of very large scale swarms of small autonomous mobile micro-robots, the ultimate goal of this research is to build sensor networks operating autonomously in open-ended environments.

Within such a swarm, micro-robots could become self-configured, self-healing, self-optimizing and self-protecting from hardware and software points of view, enabling highly scalable robotic systems able to reprogram themselves without human supervision.

Professor Serge Kernbach from the Institute of Parallel and Distributed Systems at the University of Stuttgart, Germany, is coordinating these projects and contributed, among other things to the swarm behaviour of the AquaJellies. In a paper yet to be published on collective energy management, Kernbach highlighted the emergence of specialization among a number of robots even though the whole swarm obeys to the same behavioural rules. The paper describes how the global energy efficiency of a swarm of autonomous 30x30x20mm "Jasmine" micro-robots (designed in a previous research project - see figure 9) with an autonomy of about 1.25 hours between charges varies depending on the hand-coded greed foraging strategies. The greedier (or more selfish) are each individual robots, the less efficient is the swarm for a given amount of energy resources, i.e the number of available charging stations (two copper strips, with 5V across them) where hungry robots end up queuing instead of working.

As energy becomes scarce, the need for optimisation increases. Kernbach found that the energetic performance of a swarm following a bio-inspired model nearly doubled compared to that of a swarm executing a simple threshold (charge-state) model for its robots. His

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Jasmine robots from the SYMBRION project, in what would be a very aggressive energy foraging behaviour (currently, the micro-robots have not reached this stage of coordination).

experiments also concluded that in a swarm of variable density, energetic self-regulation could be achieved through robot death (stalling short of power), increasing collective energetic efficiency. The models developed are interesting because coordination is achieved without central control and complex communication, using a very simple algorithm. Digging this further, the Jasmine robots could aggregate into more complex symbiotic organisms to reach a docking station outside their individual reach, adopting a different locomotion strategy to cross over a barrier.

At the Artificial Life Lab of the Department of Zoology from the University of Graz, researcher Ralf Mayet experiments on energy foraging efficiency with the Antbots, an adaptation of the e-puck robot developed at the EPFL in Switzerland. In a recent paper, Mayet and his colleagues have inspired their control algorithms and robot-interaction rules from ants' use of pheromone trails that give cues to other foraging ants. The experiment platform on which the Anbots operate is covered with phosphorescent paint. The Anbots emulate the pheromones trails thanks to onboard coloured LEDs that leave a glowing trace of light on the floor. Proximity IR sensors on the devices can measure the distance between the robot and obstacles, and a colour CMOS camera helps identify other robots, the food source, the nest (all colour coded with LEDs), or a light trail in-between the two. With this setup, the researcher was able to demonstrate a better efficiency in finding food and carrying it back to the nest using trails, than without the pheromone emulation. The use of an artificial sun also proved to be a very cost-effective solution to get directional information inside of a robot arena. In future developments, the robots could work in tandem to optimize speed and to minimize collisions.

As a follow up and initiated in April this year, the Collective Cognitive Robots (Co-CoRo) project involves the universities of Graz (Austria), York UK), la Superiore di Studi Universitari e di Perfezionamento Sant'Anna

(Italy), Universität Stuttgart (Germany) and the Université Libre de Bruxelles, Belgium. Running until 2015, the project aims at creating a swarm of interacting, cognitive, autonomous underwater robots able to interact with each other to balance tasks and exchange information. It is anticipated that the cognitive-based scheme used in such a swarm would allow for very fast reaction times of the whole collective system, like in a fish school. ■



The Anthots of the Artificial Life Lab from the University of Graz, emulate pheromone trails with phosphorescence.



Prototype controller achieves

over 2.6 million steps per revolution

Danish technology company, PCBMotor ApS, recently set a new performance record in printed circuit board (PCB) motors. In an experiment using its latest controller prototype, the company applied short micro-pulses (upulses) to drive the motor and achieved a record 2.6 million equivalent steps per revolution.

"We've known for some time that PCBMotors are capable of realizing very high resolutions. And now we've proven it," says Henrik Stæhr-Olsen, CEO of

PCBMotor. "The driver sets the limit for what can be achieved and we can now show that resolutions over 2.5 Million upulses per revolution are possible," says Henrik Stæhr-Olsen.

The recently conducted experiment consisted of twenty 100 upulse bursts, initiated manually via a USB connection to the motor controller, which resulted in the movement of a pointer, with a needle attached, against a linear code strip mounted on a ruler. "The resulting 2000 upulses moved the needle seven

ruler-lines which equates to 2850 000 µpulses per revolution," explains Henrik, referring to a video of the experiment that documents the results. The prototype controller, built

specifically for the experiment, is powered from the USB port and handles a wide range of settings for the motor such as pulse length and interval, drive voltage, and the number of upulses and digital steps. Operating in open-loop mode it also has on-board memory (EEPROM) for storing the drive settings. When in position, the PCBMotor and driver can be completely

powered down, removing all



mechanical and electrical interference (noise). The available holding torque depends on the size of the motor and is typically 35 Nmm for a standard 30 mm motor. PCBMotor's patented technology integrates highly accurate motors and the motor controller directly onto a printed circuit board.

PCBMotors

www.pcbmotor.com

Linear actuator

features integral connector option

Haydon Kerk Motion Solutions released the SplineRail, a motorized linear actuator with an integrated connector. Offered alone or with a harness assembly, the connector is RoHS compliant and features a positive latch for high-connection integrity. The integral connector is rated for up to 3A, and the mating connector will handle a range of wire gauges from 28 to 22 gauge. This configuration is well suited for



users who want to plug directly into a pre-existing wire harness. The SplineRail combines mechanical drive, guidance, and a stepper motor actuator in a single, compact component. The system uses a Size 17 single stack or double stack stepper motor with either a 1.8 or 0.9 degree motor step angle. Screw leads are available from 1.27 to 30.5mm per revolution, providing a wide range of performance profiles that include self-locking threads, which can support a load without external power or breaks. The SplineRail technology uses a Kerk precision rolled lead screw, supported by bearings and contained within a concentric aluminium spline, driving an integrated Kerkite composite

polymer nut/bushing. The extruded aluminium spline offers excellent torsional stability. KerKote TFE coating and selflubricating Kerkite nut/bushing material ensure long life and zero maintenance. Typical applications include pick-and-place mechanisms and robotic assemblies in life sciences instrumentation, semiconductor equipment, business machines, packaging and assembly.

Haydon Kerk Motion Solutions

www.haydonkerk.com

Design contest challenges engineers

to 'make it' creative

Freescale Semiconductor has announced the Make It Challenge design contest, which is set to take place at the Freescale



Technology Forum (FTF) June 20-23 in San Antonio, Texas. The contest will challenge attendees

to develop and submit a unique sensor robotic or system design based on Freescale's latest sensor development kit in the form of a walking robot or the Freescale Tower System.

To coincide with the contest. Freescale has introduced a sensor development kit and new Tower Mechatronics Board that contestants will use for their designs. The Tower Mechatronics Board enables designers to write software for a variety of sensor applications. When used in the Freescale sensor robot, the Tower board is capable of making the robot walk and respond to touch, motion, vibration and other external stimuli. The Freescale robot is a nine-inch tall, four degrees of freedom bipedal walking robot, with a 32-bit 'brain' and a three-axis accelerometer for balance.

To be eligible to participate in the challenge, contestants must attend FTF and complete an online course and quiz or one of two training courses offered at the forum. The Make It Challenge will have two tracks: Mechatronics Robot Track; Tower System Track.

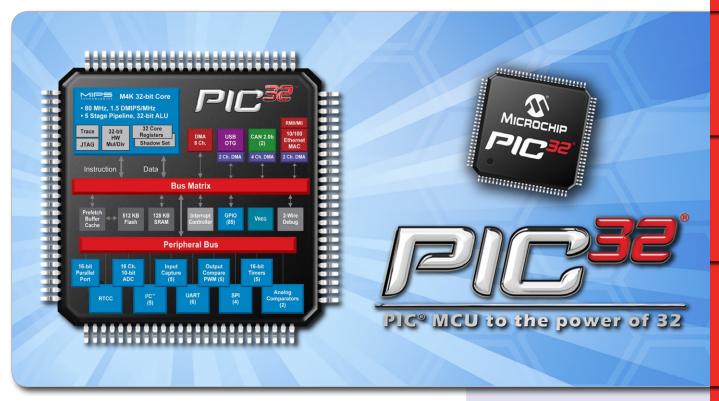
The challenge is limited to the first 200 registrants (100 per track), and participants can

choose to enter one or both tracks. Each contestant in the Mechatronics Robot Track will receive the Freescale robot (FSL-BOT) that contains the Tower Mechatronics board (TWR-MECH), as well as FSLBOT code. Participants in the Tower System Track will receive a Tower System kit containing one controller module selected by the participant. Contestants in both tracks will have access to the onsite FTF Make It Lab, where they can work on their designs and interact with Freescale technology experts.

Freescale Semiconductor

www.freescale.com

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Enabling a third dimension in user control of electronic devices

By Klaus Zeyn

TOUCHPADS WERE INTRODUCED as

notebook user interfaces in the early 1990's. Today touchpads have largely replaced trackball and isometric joysticks. Their technology has been upgraded to capacitive sensing, and their functionality now includes multitouch. But despite numerous advances over the last 20 years, touchpads limit notebook manufacturers in their design freedom due to restricted placement options and a pad depth requirement of about 5 to 7mm. In addition, a touchpad is a two-dimensional (2D) input device only.

One approach that helps overcome such limitations is to use an electrical near-field (E-field) sensor and processor that generates a localized electrical field in which it can detect anything from one-dimensional (1D) touch all the way through to complete three-dimensional (3D) gesture recognition. Developed by IDENT Technology, GestIC is a

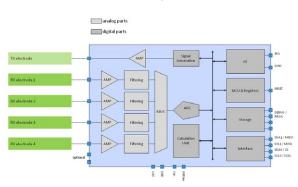


Fig. 1: IDENT Technology's GestIC SoC block diagram.

system-on-chip (SoC) that provides contactfree position tracking and gesture recognition together with control capability - see figure 1.

To sense the presence or motion of a user's hand or fingers in its vicinity, GestIC is connected to sensing electrodes which define the available sensing area as shown in figure 2. The electrodes are made of very thin low cost conductive material which can be invisibly integrated into a notebook's keyboard area. This completely eliminates the need for a touchpad as an input device, since user

Klaus Zeyn is vice president of sales and marketing at IDENT Technology AG - www.ident-technology.com

gesture recognition is used instead. The product outcome, a unified keyboard and input device (named OverKey3D), provides the position and selection control function within the keyboard area itself. Removing the need for an integrated touchpad, manufacturers are given more design options for smaller and slimmer device housings.

In comparison to touchpad-based notebooks, where users must move frequently from the key to the touch area for position or selection operations, OverKey^{3D} allows users to keep their hands conveniently over the keypad area the whole time, reducing wrist fatigue. While the solution supports position control in free space, a typical user mode for position operations is to have the hand glide

> directly on the keyboard's surface, i.e. the keys. Pending user selection, a relative or absolute x/y position control is provided with a resolution of up to 200 dots/cm.

Selection operations may still be conducted through physical buttons for familiarity, but in general they can be realized via the GestIC chip's touch sensing capabilities. Since the GestIC generated E-field works centrically over the whole sensing area with

no detection blind spots, the entire electrode area can act as a 2D touch sensing zone. Special virtual buttons can be assigned to specific co-ordinates within the sensing area. Selection operations such as click or double click are detected as the simple lift-and-tap gesture of a finger. An overall reduction of state transitions required for common operations can be achieved, resulting in faster interaction speed for users.

Another interesting feature of the gesture control chip is its ability to activate key-backlight control by instantly switching key-LEDs on and off based on the presence of a user's hand or finger. This eliminates the need to press a key to wake up the system, increasing

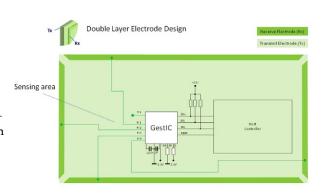


Fig. 2: Basic system level diagram of a 4 receive channel frame shape electrode connected to GestIC SoC.

user convenience and reducing overall power consumption since an LED-off signal is no longer timer based.

3D gesturing for input devices

While the advantages described above can be realized using the 1D and 2D capabilities of the GestIC chip, the really disruptive evolution arises through the chip's ability to detect and track the position of a user's hand in 3D space, turning an OverKey^{3D} notebook into a real-time 3D user input device as shown in figure 3. The GestIC chip enables this 3D motion recognition, offering an on-chip gesture library and calculating a user's motion with a responsiveness of up to 300 positions/second. Since the typical speed of a quick human motion is about 1m/s, more than sufficient data points are being recognized by the chip to perform any type of gesture and input command.

The SoC's integrated processing core can pre-process gesture inputs to provide the notebook's CPU with either x/y/z position data, simple gesture "words" or more complex dynamic gestures. Gesture events can be assigned to common user operations such as page flipping, scrolling, command calls etc. either by the manufacturer or eventually by the user himself through an OverKey3D control panel. 3D objects manipulations such as spin, zoom and rotation can be performed concurrently, without the need to stop by using keyboard commands or through a software control panel. Dynamic gesture detection in the z-direction can be used for zooming functions in new applications such as level based sub-menu navigation. Using a third dimension in user inputs makes operations faster, simpler and more intuitive.

Notebook manufacturers are currently seeking human-machine interface (HMI) innovations in order to respond to the recent shuffle that tablets caused in the mobile PC market. The OverKey^{3D} solution addresses this need, elevating HMI options for notebooks from traditional selection and 2D positioning to the next level, enabling the 'third dimension' of 3D free space gesture recognition for user input operations.

The GestIC chip evolved from IDENT's mass market proven and patented Z-Sense technology pool. Z-Sense is an electrical near field sensing technology using a carrier frequency of about 100kHz, corresponding to a wavelength of about 3km. Since the distance between the electrodes is only a tiny fraction of the wavelength, the magnetic field component and radiated energy is practically zero, resulting in a pure quasi static E-field that does not interfere with mobile radios. Furthermore, the E-fields generated are independent of ambient influences such as light, sound, skin color, humidity, etc. In



Fig. 3: Notebook with OverKey^{3D} functionality.

contrast, other 3D input technologies such as optical, ultrasound or infrared systems are negatively impacted by such environmental influences.

In comparison to optical systems, which are facing angle related coverage issues in near range and consume typically over 500mW of power for a simple set of 3D functionality at a responsiveness of 50 frames/s, the GestIC solution requires less than 10 percent at significantly higher update rates. Designers with constant pressure on short

design cycles can benefit from GestIC's flexible SoC architecture with on-chip processing and on-chip gesture library.

Quick-turn solutions can enable rapid time to market, and investments are protected due to a flexible memory architecture supporting in-field upgradability of the device. IDENT has already built OverKey3D demonstrators based on off-the-shelf keyboards. This functionality is now being also transferred into smaller devices such as mobile phones.



Gaming moves to efficient context awareness with more sensors

By Stéphane Gervais-Ducouret

GAMING, supported by electronic devices, has expanded from a niche market to encompass age categories from toddlers to seniors. One enabler of the explosion of gaming adoption is an intuitive user-interface, as used by the Wii and motion games on phones or MP₃ players.

Intuitiveness of action through gesture is possible because of sensors like accelerometers and gyroscopes, which use Micro Electro Mechanical Systems (MEMS) technology with analogue mixed-signal chips in one package. They benefit from low-power consumption, small real estate, easy implementation and low price per unit.

The aggregation of different sensors like accelerometers, gyroscopes, e-compasses and altimeters with the adequate software enables the development of advanced games such as piloting a drone or interacting with a robot. However, the vast majority of the games played on portable devices use only one or two sensors: generally accelerometers and capacitive touch sensors. The rate of adoption by the end user is so high that it is common to see people touching the screen or shaking their new portable device when experiencing a game. The success of such games is based on the simplicity of control allowed by the sensors. What's more the main sensor used in these games, the 3-axis accelerometer, has gone through a tremendous evolution. Analogue output motion sensors like Freescale semiconductor's MMA7261QT accelerometer, provide continuous information about user movement such as acceleration with a 6-bit ADC precision and are still used in console accessories. However, smarter devices with embedded functions are invading the portable and mobile electronic device space. Automatic sampling rate, interrupt control, pulse and jolt detection, low-power consumption, digital interface and high precision with a 14-bit like Freescale's MMA8451Q accelerometer are staples of embedded functions. Such

Stéphane Gervais-Ducouret is global marketing director for sensors at Freecale Semiconductor - www.freescale.com

parts enable very accurate gesture recognition without the penalties of power consumption. New games providing novel user experience by reflecting the complexity of hands gestures are starting to emerge thanks to these new capabilities.



Fig. 1: MMA9550L with a 3-axis magnetometer for a pointing device application.

Despite the considerable adoption of games using sensors in portable devices and games console accessories, the association of gaming and sensors is still in its early stages. Sensors are adding new dimensions which are unlocking innovative fields. For instance, Freescale has leveraged its medical know-how to adapt it to new games based on "emotion sensing". The platform uses a standard console game controller with the implementation of sensors like capacitive touch, humidity, accelerometer and pressure. The data of each sensor is processed through a 32-bit MCU with specific software developed based on neuroscience theories and experiments: heart rate, sweating, muscle contraction and attitude reflect a person's emotion. By analyzing these parameters in real time, the game can reflect the player's emotion with real life interaction. One of the demonstrated games is a sniper shooting game where the shooting becomes more difficult depending on the detected emotion of the player: for instance, with a shakier target if the player is getting upset or a lower visibility if the player is sweating. This type of interaction makes any game much more interesting since each session is adapted to the player and reflects the player's feelings more accurately. With such an approach, the number of gaming possibilities becomes exponentially proportional to the number of sensing elements; and creating interfaces for such games becomes increasingly complex-

Adding new kinds of sensors and combining the pre-processing and fusion of their

data input is the current challenge for new applications. For this purpose, Freescale has developed a new concept which combines a microcontroller with a motion sensor within the same package (the MMA9550L motion sensor platform, part of the Xtrinsic family). This motion sensor platform provides not only the extracted and pre-processed data of the motion sensor to the main application processor, but can also combine and conduct fusion of data together from external sensors. Consequently, specific sensor complexity like calibration, data filtering and specific application data is moved to this local MCU and only the required data is provided to the developer for easy implementation. Using this new product concept, a call to a highlevel programming function is enough for a developer to access the data he/she wants.

A simple example for a pointing device application (acting as an air mouse) is shown in figure 1. A standard solution uses a 3-axis accelerometer and a 3-axis magnetometer which requires two different digital interfaces connected to another microcontroller or application processor. The magnetometer calibration (soft iron and hard iron) has to be managed by an external processing resource. The tilt compensation, using the accelerometer information, must also be processed. So, 3360 bit/s of raw data needs to be calibrated and processed (assuming a sampling data rate of 60Hz for each sensor). Using Freescale's MMA9550L, the 3-axis accelerometer can be replaced by adding processing power and interfaces for external sensors; it also has the same real estate size: 3x3mm.

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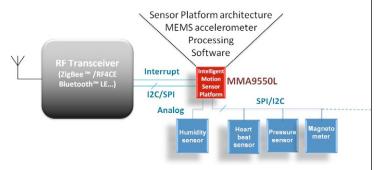


Fig. 2: Example of a richer sensor context in a special wireless gamepad.

Therefore, still working with a presumed data rate of 60Hz, the magnetometer calibration and tilt compensation can be locally processed with only 640 bit/s of processed data. The data provided can be used directly by the game developer. Beyond this gain in data processing, power consumption is reduced. Since we also avoid synchronization issues and task scheduling, real time reactivity is greatly improved due to lower data latency. This adds to the time savings on data processing.

By extension, using sensors connected wirelessly opens up the path to a new generation of games where the real world can be viewed through wireless sensor networks (WSN) and visualized through virtual reality. The bottleneck of processing all the data coming from the sensors can be solved by using intelligent sensors like the MMA9550L, since local processing will greatly reduce the main application processor CPU usage and data loading. Re-creating a certain reality through different kinds of sensors like cameras,

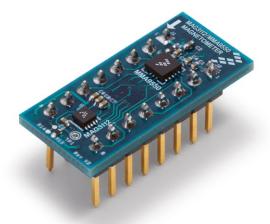
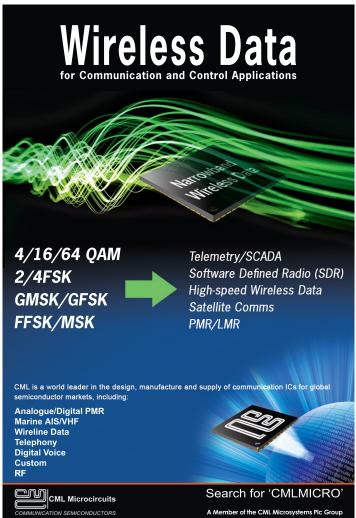


Fig. 3: MMA9550 and the magnetometer MAG3112 in a 3-axis ecompass module.

accelerometers, capacitive touch, and gyroscopes is going beyond simply adding a third dimension to the image, as it allows for an interpretation of the reality. Players may be able to enter an era of "contextual interaction" whereby real world interactions can help the player control the game rather than the player having to adapt to the game.

An illustration of a richer sensor context in a special wireless gamepad is shown in figure 2. Processing the sensor data before transmission is important for real time processing and to achieve the best trade-off for power consumption, communication and computation. Combining the input of a high accuracy accelerometer with the processing enables designers to adapt the sampling rate from 1Hz, when no activity is detected, to a few kilo-Hertz of data sampling when user activity is at its maximum. The future is in contextual interaction, supported by a network of sensors that allows gamers to interact with a number of parameters from their surroundings.





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The 'internet of things' is driving demand for mixed signal MCUs

By Philip Ling

THERE IS INCREASED activity around the 'internet of things'; the ability to create networks of small devices that monitor and control our surroundings to create a sort of 'augmented reality'.

A recent development is NXP's intention to open-source its JenNET IP protocol stack, which uses the IEEE 802.15.4 MAC and PHY as its underlying platform and employs the IPv6 protocol to extend the network's addressable nodes to what is often termed as 'effectively limitless'. It is this potential to give any electronic device its own IP-addressable profile that will lead to the 'internet of things' concept becoming reality.

However, in addition to uniquely identifying these 'things', it follows that the 'things' should do something useful and, increasingly, the application that is most often cited is monitoring and control. Consequently, data gathering using some form of 'smart' sensor is expected to constitute a large part of activity for the 'internet of things'.

A market report by analyst IDC and cited by Intel states that by 2015 there could be 15 billion devices with an embedded internet connection, more than two for every single person on the planet today. In reality, as smart sensor applications flourish, the number of connections could grow beyond this figure rapidly, and that will be enabled in large part by the falling cost of developing and deploying connected devices. A major element of that cost will be the embedded intelligence and it is here that many IDMs are focusing their attention, in developing low power, low cost MCUs that meet the commercial and technical requirements of this emerging application space.

Mixed signal MCUs which also integrate wireless connectivity are already available, they will likely become more prolific in the future. However, for many applications, integrating the wireless connectivity may be less appealing than a two-chip solution, at least while the battle over which wireless protocol will prevail still rages. For this reason, perhaps, there is more activity around developing ultra-low power MCUs that focus on interfacing to ever smarter sensors.

Marking its entry into the MCU market, ON Semiconductor recently introduced its first mixed-signal MCU which focuses on applications that demand precision, as well as low power. ON Semiconductor recently acquired Sanyo Semiconductor and, with it, a portfolio of 8 and 16-bit MCUs. However, for its first in-house development, ON Semi chose the ARM Cortex-M₃ 32-bit core, which it has married with some mixed signal elements to create the Q32M210. It claims the device has been developed to target portable sensing applications that require high accuracy, predictable operation and the ever-present power efficiency.

ON Semi is more accustomed to developing custom ASICs rather than its own products, however through a number of other acquisitions it believes it has accrued the expertise necessary to address the needs

of 'niche' applications, where precision is valued. It is the company's experience in developing niche mixed signal products that forms its credentials, not least in the development of hearing aids that use highly accurate ADCs and a bespoke DSP technology.

The analogue front-end (AFE) used in the Q32M210 features dual 16bit ADCs and configurable op-amps, which

result in a true ENOB of 16bits across the power supply range. This is enabled, in part, by an uncommitted charge pump that can be used to extend the operational lifetime of the battery supply. ON Semi claims the charge pump can be used to deliver a consistent 3.6V to the AFE, even when the battery supply has dropped to 1.8V. This could significantly extend the usable lifetime of any device empowered by the Q32M210.

The additional peripherals provide a USB interface, as well as LED/LCD drivers and push-button interfaces. Coupled with the programmable sensor interface, this positions the device as a system-on-chip solution for a range of applications and specifically



Energy Micro has recently introduced the first Gecko device to feature its sensor interface technology.

portable medical devices, where its accuracy will be valued.

The AFE used in the Q32M210 is clearly intended to differentiate it from the competition, in terms of both accuracy and power consumption. However ON Semi isn't the only device manufacturer to acknowledge the importance of mixed signal performance. Energy Micro, which also uses the Cortex-M3 core in its ultra-low power mixed

> signal MCUs, has recently introduced an architectural feature that is set to appear on a number of devices in its family and is currently available on the Tiny Gecko EFM32 range.

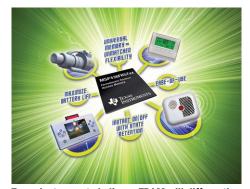
The LESENSE interface is one of the Gecko's autonomous peripherals, meaning it is able to continue operating while the ARM core is in a deep sleep mode, thereby saving energy. Up to 16 sensors can be monitored and stimulated using just the LESENSE

interface, which also features a configurable state machine with up to 16 states, acting as a decoder that can store the results in a buffer, ready for the core to retrieve at a predetermined interval. This avoids waking the core to perform regular 'house-keeping' sensor measurements.

Each of the 16 channels has its own set of configuration registers. The scan sequencer runs from a pre-scaled version of the system clock and each channel cycles through three phases; idle, excite and measure, the length of the latter two are configurable through the channel's timing register. Excitation of the sensor, if necessary, can be through either driving the corresponding pin high,

ON Semiconductor's first own-brand MCU offers precision mixed-signal capabilities with an ARM Cortex-M3 core.

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Texas Instruments believes FRAM will differentiate its MSP430 in sensor-based applications.

low or connecting it to the output of a DAC channel.

Sensor evaluation can be either an analogue comparator or a counter output, with the output being used to trigger an interrupt. One application example shows the interface being used to driver four capacitive touch-buttons, which are scanned at 100Hz (100 times per second), triggering an interrupt if one of the buttons is pressed.

This clearly targets a different application area from ON Semi's precision mixed signal MCU, however it highlights the need for relatively simple sensor monitoring in applications such as user interfaces, and more complex applications where specialist sensors are used, such as equipment used to monitor a combustible environment, a smoke detector or temperature monitoring.

A further aspect to the proliferation of sensors is the increased acquisition of data; data which may need to be stored and updated frequently. In these applications the use of Flash as a data storage medium may be challenging, at least that's what Texas

Instruments believes. While Flash has many benefits, it also comes with relatively high power demands in comparison to non-volatile memory. However, clearly non-volatile memory also faces the issue of data loss when power is removed and in a bid to address this problem, TI has developed an all-FRAM version of its low power 16bit MCU, the MSP430.

FRAM, or ferro-electric RAM, has been in development for some time and there are a number of standalone FRAM memory devices available, however this is the first time it has been used in an MCU targeting ultra-low power applications.

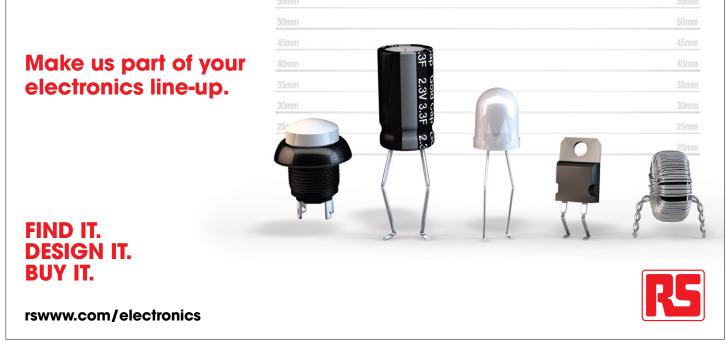
Specifically, FRAM is suitable for smart sensor applications because it offers a much faster write time than Flash, with much higher read/write endurance. For the MSP430, the difference is significant; the new device can achieve 1400kbyte/s write times with the FRAM device compared with just 13kbyte/s for Flash. This translates to much less time - and therefore energy - used to store data. And while the read/write endurance for Flash is around 10k cycles, it is 'virtually limitless' for FRAM.

So the question is, why hasn't FRAM displaced Flash in this and other application areas? The reasons are, perhaps predictably, more commercial than technical. Even though it has fewer additional manufacturing processes than Flash (two for FRAM as opposed to five or more for Flash), manufacturing FRAM only makes economic sense at 130nm and even then only up to a density of

around 512kbyte. Beyond that, it still costs less to use Flash, which is why this first FRAM family has been squarely aimed at the smart sensor application space, where the need for density is still modest.

Interestingly, while FRAM is being promoted as a unified memory solution, capable of replacing Flash, SRAM and DRAM, the MSP430FR57xx range will still integrate an amount of SRAM and the reasons given are twofold; existing applications that use SRAM will be easier to port to FRAM devices that retain the same memory architecture, and secondly TI admits that using SRAM can overcome the timing limitations of FRAM when executing directly from memory. That said, the FRAM's performance can maintain a clock speed of 8MHz without wait states, which rises to 24MHz when the SRAM cache is used. However, FRAM scales with the technology node, so TI firmly expects this speed to increase in future. A further concession is the inclusion of on-chip ECC which isn't supposed to be necessary for FRAM, but is included here to provide a 'safety net' for customers.

While the MSP430FR57xx doesn't feature the same level of mixed signal capability in terms of a dedicated sensor interface as the other devices covered here, it does offer up to 12 ADC channels and is clearly going after the same applications. In future there will be even more mixed signal MCUs aimed at this expanding application area, providing further opportunity for developers targeting the 'internet of things'.



SAR ADCs control the world

By Guy Hoover

DESIGN GOALS for today's industrial control systems demand that systems are faster, more accurate and smaller, while consuming less power and providing greater reliability. Designers of these systems must choose components that ensure that these goals are met. One of the central components in an industrial control system is the analogto-digital converter (ADC).

System designers have several types of ADCs to from which to choose, including pipeline, delta-sigma and SAR (successive approximation register) architectures. Without getting into the details of how each ADC works there are several characteristics that must be considered when selecting an ADC. Pipeline ADCs are capable of very fast conversion times, can digitize very fast input signals with low distortion but draw high supply currents, have poor signal-tonoise ratios (SNR) and pipeline delays (a delay of a fixed number of samples between the instant the input is sampled and the time the data is available). Poor SNR can be overcome with averaging at the expense of lowering the effective sample rate. Pipeline delay obscures the real-time nature of the data, making fine tuning of control loops difficult. Delta-sigma ADCs excel in applications requiring high precision and low noise, but their low sampling rate limits their use to applications near DC. SAR ADCs are capable of conversion rates from a few megahertz down to DC and can handle input signals from DC to tens of megahertz with good SNR and low distortion. SAR ADCs can sample on an as needed basis and then deliver that data without any pipeline delays, providing timely feedback for control systems, resulting in a tight control loop with good transient response.

One example is the LTC2379-18 from Linear Technology, a 1.6Msps, 18-bit SAR ADC that consumes only 18mW. The 16-pin 4x3mm MSOP device operates from a 2.5V supply and has a fully differential input range of +/-2.5V to +/-5.1V that is set by Vref. With a guaranteed total harmonic distortion (THD) less than -115dB, a signal-to-noise ratio greater than 98dB, integral nonlinearity (INL) less than 2LSBs, no missing codes at 18-bits and guaranteed operation up to 125°C, the LTC2379-18 provides the speed, accuracy, low power consumption and reliability required by today's control systems.

The finer grained control required by modern systems necessitates the ability to measure smaller time increments. This ability to measure smaller time increments, in a real-time loop, is limited by the ADCs' maximum sampling rate. The maximum sampling rate is inversely related to the sum of the ADC conversion time and acquisition time. Serial ADCs are usually thought of as being slower than parallel ADCs because of the time required to shift out the data. In the case of a serial ADC the data is usually transferred during the acquisition period. If the data transfer time is less than the acquisition time then the serial ADC's maximum sampling frequency is no slower than a parallel ADC with similar conversion and acquisition times. The LTC2379-18 has a minimum acquisition time of 200ns, which is approximately the same as the minimum data transfer time of 18ons, indicating this part is optimized for maximum sampling frequency.

Guy Hoover is applications engineer, mixed signal products at Linear Technology - www.linear.com

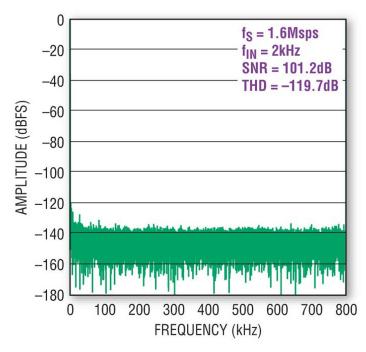


Figure 1: 32k point FFT shows low distortion and noise of LTC2379-18.

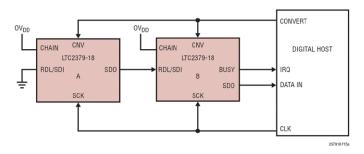


Figure 2: LTC2379-18 CHAIN mode allows multiple ADCs to communicate with host processor using only four wires.

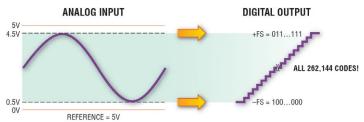


Figure 3: LTC2379-18 digital gain compression shrinks analog input span while maintaining full digital output span, allowing single supply driver operation.

That same need for finer grained control also necessitates higher accuracy in control systems. When moving up from 16-bit to 18-bit performance, it is important to look at more than just the number of bits. Don't be fooled by "marketing bits." Make sure that the ADC is specified with no missing codes over the full temperature range. An ADC with good SNR provides more noise margin when making measurements, which reduces the need for averaging. Less averaging

DESIGN&PRODUCTS

results in control loops with smaller delays, making them more stable. DC applications require good INL and DNL specifications, while AC applications require a good THD specification. The FFT of figure 1 shows the typical performance of the LTC2379-18, which includes SNR of 101.2dB and THD of

The LTC2379-18 is compatible with the SPI standard and is capable of interfacing with 1.8V, 2.5V, 3.3V and 5V logic families. A daisy chain mode shown in figure 2 allows multiple LTC2379-18s to share the SPI and Busy lines, which is useful in instances where large numbers of converters might otherwise make the number of signals required impractical. Chain mode is also useful when synchronizing the data from several channels, which is necessary for maintaining phase information between channels. The Busy line can be eliminated if the digital host is able to wait the maximum conversion time before starting the data transfer, further reducing the line count from four to three.

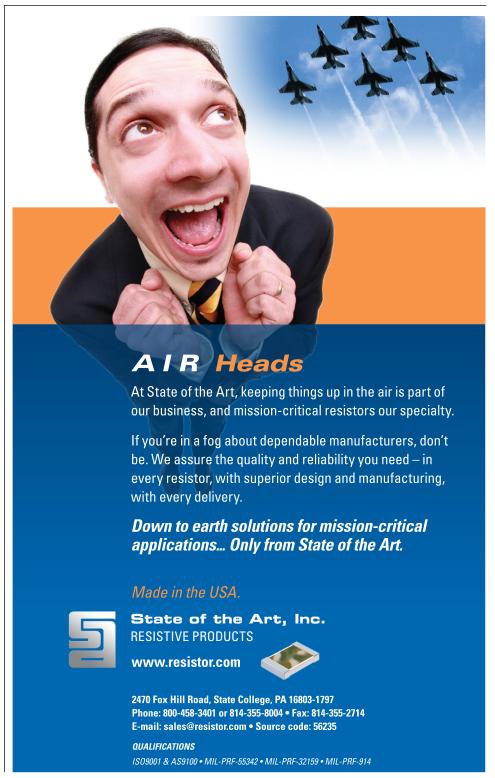
As control systems become more complex and the number of channels increase as space requirements shrink, reducing system power demands becomes more important. In addition to shrinking operating costs, reducing power requirements also simplifies thermal management. Selecting components with built-in power management features makes reducing power easier. As an example, the LTC2379-18 automatically powers down after a conversion, resulting in even lower power dissipation at low sample rates.

Single supply ADCs usually have an analogue input range that ranges from ground to Vref. Due to driver headroom requirements, this means that the driver driving the ADC requires a supply voltage at least a few hundred millivolts greater than Vref and a negative supply a few hundred millivolts below ground. This is true even with rail-torail drivers because distortion increases as the output nears the plus or minus supplies. Until now this meant either running with a single supply and throwing away thousands of codes near ground and V+ to keep distortion low or running on a split supply and consuming more power.

A digital gain compression feature, available on the LTC2379-18, allows a zero to full-scale ADC output swing to be achieved with an input that ranges between 10% and 90% of the +/-Vref analog input voltage. For a 5V reference, this means that the analog input range is 0.5V to 4.5V while still main-

taining all 262,144 output codes, as shown in Figure 3. Compressing the analog input range gives the ADC driver more headroom above ground and below the positive supply voltage. This feature allows the LTC2379-18 buffer to be powered from a single supply, resulting in significant power savings.

Reliability is one of the most important goals in designing control systems. Customers want to buy reliable products. Increasing noise margins, making more accurate readings, reducing the number of signal lines and power supplies, lower power consumption and good thermal management all make for a more reliable system. The selection of high quality components, including the ADC is equally important. Care should be taken to ensure that all critical ADC specifications such as INL, DNL, SNR and THD are fully guaranteed, not just typical specifications.



Equally important is that the specifications be guaranteed over the full temperature range in which the system must operate.

The LT6350 can be used to buffer and convert large true bipolar signals which swing below ground to the ffl₄V differential input range of the LTC2379-18, with digital gain compression enabled in order to maximize the signal swing that can be digitized. Figure 4 shows the LT6350 used to convert a ffl10V true bipolar signal for use by the LTC2379-18. In this case, the first amplifier in the LT6350 is configured as an inverting amplifier stage, which acts to attenuate and level shift the input signal to the 0.5V to 4.5V input range of the LTC2379-18. In the inverting amplifier configuration, the input impedance is set by resistor RIN. RIN must be chosen carefully based on the source impedance of the signal source. Higher values of RIN tend to degrade both the noise and distortion of the LT6350 and LTC2379-18 as a system. Lower values of RIN may be difficult for the signal source to drive. The resistors on the inputs of the first amplifier in the LT6350

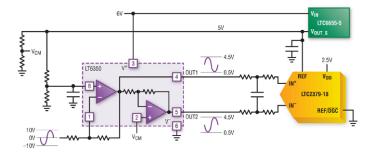


Figure 4: LTC2379-18 and LT6350 accept a ±10V input signal while running off a single 6V supply.

must be selected to achieve the desired attenuation, common mode output voltage and to maintain a balanced input impedance. The circuit of Figure 4 has an SNR of 99dB and a THD of -95dB. ■

Novel harmonic analysis method for smart metering

By Petre Antonesei and Gabriel Minciunescu

WITH WIDER DEPLOYMENTS of smart metering, smart grids and distributed generation, power quality monitoring has become of great importance. Harmonic analysis of current and voltage signals allows several key power quality indicators. For example, an energy meter with harmonic analysis functions can characterize the state of the load or supply, enabling predictive maintenance or system optimization.

The presence of harmonics is an ever increasing concern for providers and consumers of energy alike. Excessive harmonic currents can lead to overheating of power transformers and reactive power compensators and neutral conductors. False tripping of protective relays can also be caused by harmonic currents. Harmonic voltage and currents can also interfere with sensitive equipment operating in proximity to large harmonic generators. Traditionally developers would use a digital signal processor to implement some version of the Fourier algorithm or bandpass filtering to perform harmonic analysis. This article presents a new approach, titled Adaptive Real Time Monitoring (ARTM) and compares it against other possible methods: FFT

Petre Antonesei is systems engineer and Gabriel Minciunescu is senior DSP design engineer, both work at Analog Devices - www.analog.com

algorithms and bandpass filtering. ARTM will be featured in the next generation Analog Devices (ADI) products for energy applications.

Fourier based methods

In energy metering or power quality monitoring systems, when the harmonic analysis is performed, phase currents and voltages are simultaneously sampled and then processed to compute the following power quality measurements on the fundamental and harmonic components: active, reactive and apparent powers, rms values, power factors, and harmonic distortions. Fast Fourier Transform (FFT) analysis comes immediately to mind. The procedure requires the following steps as in figure 1.

One must determine the period of the fundamental component. This can be a time consuming process that is typically realized by low pass filtering the phase voltages to isolate the fundamental and measuring the time between consecutive zero crossings. Any error in determining the period propagates to the error in amplitude and phase of the harmonics.

The sampling frequency must be modified to obtain 2N samples per period. This implies using analog to digital converters that allow variable sampling frequencies. Then one must acquire 2N samples corre-

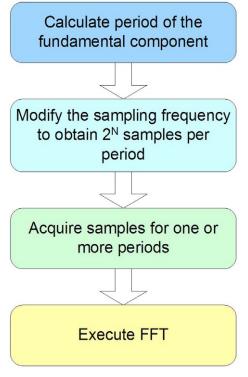


Fig. 1: Steps required to implement FFT algorithm.

sponding to one or more periods. The last step is to execute the FFT algorithm. Samples taken across multiple periods increase the accuracy of the computations. But this means a heavier burden on the DSP and a slower overall response.

DESIGN PRODUCTS

Calculate period of the fundamental component

Acquire samples for one or more periods using a constant sampling frequency

Execute Goertzel algorithm

Fig. 2: Steps to implement the Goertzel algorithm.

One can see that modifying the sampling frequency function of the fundamental period affects other calculations usually executed in an energy meter. Energy computations include a lot of filters that have coefficients computed function of the sampling frequency. Implementing an entire metering program with dynamic adjustment of such coefficients may be avoided if the Goertzel algorithm is adopted. This approach computes the DFT using a number of samples per period different than 2N, allowing for a constant sampling frequency independent of the fundamental period. The steps to implement such algorithm are as in figure

The period of the fundamental component still needs to be determined as already presented for the FFT implementation. The sampling frequency is now constant and a certain number of samples per period are acquired. The coefficients used in the Goertzel algorithm are computed based on the number of samples per period. The Fourier transform is then executed.

Bandpass filter based method

Perhaps the simplest approach to harmonic analysis is to use bandpass filtering. It basically takes the phase currents and voltages and applies a narrow band filter around one harmonic. One can analyze multiple harmonics simultaneously if multiple filters are implemented in parallel. The steps to implement this approach are as described in figure 3.

In this approach, the period of the fundamental harmonic still needs to be determined. The accuracy of this measurement needs to be substantially increased because at higher harmonics, there is the risk of missing the harmonic frequency of interest. This practically means longer time reserved

to filtering the time period between consecutive zero crossings. The filter coefficients are computed based on the fundamental period. The phase currents and voltages are filtered at the desired harmonic and the corresponding rms values are computed. One drawback of this method is that only the amplitude of the harmonic is preserved and any phase information is lost. Hence the harmonic powers, the power factors and harmonic distortions cannot be computed.

Adaptive real time monitoring (ARTM)

Since the fundamental frequency of the power grid can drift over time, there is a great advantage to a harmonic analyzer that can track these changes in frequency automatically, without the user intervention. ARTM continuously estimates the likely value of the fundamental frequency and compares it to the real frequency present on the voltage line.

Any error coming out of this comparison is used as a feedback factor to increase or decrease the value of the estimated frequency. This is basically the self-adapting element of ARTM. Based on the estimated frequency or integer multiples of it, a real-time procedure to extract spectral components is performed on the voltage and current of a selected phase. This operation will create a set of values that are proportional with the energy present at the estimated frequency (or multiples of it). By performing further signal processing operations on these values, we can provide the real-time powers and RMS values at fundamental or integer multiples of the fundamental frequency (which, in fact, are the harmonics).

For poly-phase systems, independent frequency estimators will be dedicated to each phase voltage. This way, even if the voltage of a phase goes down, the user can select one of the remaining ones to get an estimated frequency of the power grid and use it in the procedure mentioned earlier.

By controlling the integer multiplication factor, it can be decided (in a flexible manner) which harmonic will be monitored. This has the advantage of dedicating all the DSP computational resources to monitor just the harmonics of interest. By contrast, an FFT approach will be computing the values at multiples frequencies of the spectrum at once, but it will consume much more resources in doing so. To achieve the same performance levels, the memory locations needed to store a certain number of samples that will be used by the FFT algorithm are significantly higher when compared with this proposed real-time method. Monitoring a choosen harmonic will become even more powerful and relevant if the fundamental values are also monitored in parallel: it enables the computations of harmonic distortion (HD) ratios for RMS components of current and voltage, an indicator







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METHOD	Real Time Monitoring	Adaptive	DSP Memory Requirements	Accuracy	Spectral Harmonics snapshot
ARTM	YES	YES	Small	Very High	YES
FFT	NO	NO	Very large	Low	YES
Goertzel Algorithm	NO	NO	Small	Medium	YES
Bandpass filtering	YES	No	Small	Medium	NO

in real time can be very useful as a global indicator of the power quality, but also for systems trying to implement control loops aimed at keeping the power factor within given boundaries.

Another benefit of computing the active, reactive and apparent powers in real-time, is that energy values at fundamental or harmonics can be obtained

Calculate period of the fundamental component

Adjust filter coefficients function of fundamental period

Execute bandpass filtering

Fig. 3: Steps to implement a bandpass filter.

that sometimes is more meaningful than just the absolute values. In fact, from a purely theoretical DSP perspective, this is a widespread and accepted method of presenting data in a normalized fashion. In one further step, by performing a sweep of the HD values for certain range of harmonic indexes, the total harmonic distortion (THD) can also be computed by adding the values obtained.

Beside magnitude

response over frequency, a classic and complete harmonic analyzer should provide information about the phase response at certain frequencies.

The ARTM provides phase information in terms of power factor calculation which is the ratio of active power versus the apparent power. ARTM computes power factor corresponding to fundamental frequency (known as displacement power factor) but also corresponding to various harmonic frequencies. Having these values

through accumulations. This will allow the user to analyze how the total energy consumption is being distributed between fundamental and harmonic components. In 3 phase systems there is further interest in harmonic analysis of the neutral current and on the sum of phase currents, especially in the presence of triplen harmonics (odd multiples of the third harmonic) created by various non-linear loads.

Because the net effect of triplen harmonics is additive, the neutral conductor may end up carrying more current than it was designed for leading to overheating

Estimate in real-time the fundamental frequency using one active phase

Performs real-time spectral extraction for fundamental frequency and for user selectable multiples of fundamental frequency

Combine the above values from voltage and current to obtain real-time rms and power values for the fundamental and for userselectable harmonics

Fig. 4: Steps to implement Adaptive Real Time Monitoring.

and possible fire. Triplens can also cause problems in three-phase delta transformers due to circulating currents that can overheat the windings. Being able to monitor the harmonic components on the neutral current as well as on the sum of phase currents can also be useful in indicating some potential imbalance issues.

Table 1 shown above presents a comparative summary of the various methods discussed in this article. Bandpass filter and ARTM can be used to monitor the fundamental and harmonic components in real time. If the fundamental frequency of the power line changes, the ARTM method is proven to respond immediately with sufficient

The memory occupied by an eventual implementation is very large in case of the FFT (because of the need for samples storage) and quite small in the case of the other methods. The accuracy of the results is very high for ARTM, medium for Goertzel algorithm and bandpass filter and low for the FFT.



Light curtains with integrated reflector

two-colour display for error-free shelf control

With its Light Curtains Pick to Light, sensor producer Wenglor extends its portfolio of photoelectronic sensors, following the

"Pick to Light" principle whereby the light curtains monitor the correct parts picking processes in shelves and storage locations. The Light Curtains function

according to the retro-reflex principle, meaning that transmitter and receiver are integrated into the same housing and need a

reflector in order to function. The light curtains feature a reflector foil pre-mounted to the back of the sensor's housing and serves

> as reflector for the neighboring light curtain. An integrated two-color job display (green/red) indicates a correct or respectively incorrect parts-pick-

ing process to the user.

Wenglor

www.wenglor.com

Digital ambient illuminance sensor

in thin SON package

Renesas Electronics has announced the PH5551A2NA1 digital ambient illuminance sensor which features an industry-leading compact and thin package. The device is the company's first entry into the market for ambient illuminance sensors and incorporates Renesas Electronics' technology expertise accumulated in the development and commercialization of photo detector IC products for CD, DVD, and BD players. The digital ambient illuminance sensor is designed to contribute to improved performance and

reduced power consumption, for example by automatically adjusting display brightness for the best viewing experience.

The PH5551A2NA1 is a digital ambient illuminance sensor that detects the brightness of ambient light and sends a corresponding signal to a device such as a microcontroller (MCU). The PH5551A2NA1 employs a clear mold package design measuring 1.56x2.55x0.55m.

Renesas Electronics

www.renesas.eu

Signal conditioner

eases the calibration of LVDT position sensors

The Eazy-Cal from Macro Sensors is what the

company claims to be the most userfriendly LVDT signal conditioner. Employing a virtually effortless fingertip calibration routine, the Eazy-Cal MMX series saves time

and money by eliminating the repetitive null and span potentiometer adjustments associated

with conventional analog based

signal conditioners. An intuitive, sequencing four LED status indicator guides the operator through the calibration process, and provides foolproof feedback to insure calibration integrity.

Macro Sensors

www.macrosensors.com

Air pressure sensor for altitude

with very low temperature coefficient

The BMP180 from Bosch Sensortec is a new barometric pressure sensor in MEMS technology, which can accurately measure changes in air pressure. The BMP180 has a high relative measuring accuracy of 0.12 hPa combined with a low temperature coefficient and low noise. Since temperature fluctuations, for example due to a change in the ambient temperature, can occur in cell phones, the temperature coefficient of the sensor is crucial to the accuracy of the altitude measurement that is achievable in practice. The temperature coefficient of the BMP180 is o.o1 hPa/°C, the lowest on the market claims the manufacturer. Bosch has succeeded in reducing the noise

of the sensor to 0.02 hPa. This enables the BMP180 to detect altitude changes down to 0.17 m.



The BMP180 measures absolute pressure or altitude relative to a reference plane such as sea level accurate to within ±1hPa. Delivered in a 3.6x3.8x0.93mm package, the BMP180 is around 60% smaller than its predecessor.

Bosch Sensortec

www.bosch-sensortec.com



Multi-input analog measurement module

with sensor excitation up to ±15 V and ±45 mA

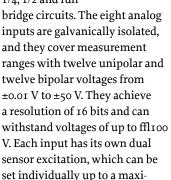
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Ipetronik has launched a fast, eight-channel multi-input analog measurement module, the Sx-STG, that supports the user's choice of one of three different signals per measurement

input: voltage, integrated circuit piezoelectric (ICP) sensors, and Strain Gauge (STG) sensors for measurements on 1/4, 1/2 and full



mum of ±15 V with up to ffl45 mA. An 8th-order, 4,800-Hz Butterworth filter that can be turned on and off has been integrated as the hardware filter. The module offers channel sample rates be-

> tween 1 Hz as and 40 kHz. Four different rates can be selected per module. Measurement data output is accomplished via Ethernet at a maximum speed of 100 MBit/s in accordance with IEEE 802.3

via XCPonEthernet (UDP/IP). Due to the use of a dual bus concept (CAN and Ethernet in a single cable), it will also be possible to output the measurement data directly to the CAN bus at a sample rate of up to 2 kHz once system integration is complete.

Ipetronik

www.ipetronik.com

to design around Freescale's Kinetis K60 MCUs



Earlier this year, IAR Systems launched a complete development kit for Freescale Kinetis K60 family of MCUs and modu-

lar Tower System. In this month's reader offer, the company is giving away four such kits worth 190 Euros. The modulebased kit includes

hardware boards, debug probe, software tools and code examples. The package includes the Kinetis K60 MCU module with on-board K60N512 32-bit microcontroller, a serial peripheral module with connectors for editions are included in the kit Ethernet, USB, CAN, and other connectivity. The Kinetis K60 MCU module features capacitive touch pads, SD card slot, 3axis accelerometer, buttons and a potentiometer. An additional

prototyping module provides a large area where a wide range of applications can be evaluated. Target connection is provided

> by the IAR J-Link Lite for Cortex-M debug probe that is included in the kit. It allows SWO debug-

ging including SWO trace that can be used for execution time analysis and visualization of variables and interrupts in the debugger. IAR Embedded Workbench KickStart and Evaluation for software development. The KickStart edition has a 32k code size limit and the Evaluation edition is a fully functional version limited to 30 days.

IAR Systems

Check the reader offer online at www.electronics-eetimes.com www.iar.com

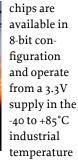
Ferroelectric RAM chips

ready up to 256kbit

OKI Semiconductor (part of the ROHM Group) is developing a new memory technology called ferroelectric RAM (FeRAM) that extend the company's memory line-up already consisting of

EEPROM, DRAM and P2ROM. FeRAM is a nonvolatile memory that uses a ferroelectric film as a capacitor for data storage. Compared to other non-vola-

tile memory as EEPROM and Flash is has the advantage of a much lower power consumption (1:400 or less), a high-speed writing (similar to DRAM) and a significant higher number of writing cycles (1012 times). Together with the data retention of 10 years these features enable engineers to use FeRAM in many applications, where a reliable storage of data is mandatory such as accounting, configuration and status information in consumer, industrial and car multimedia applications. The



range. The current line-up include 32kbit density with SPI I/F in a SOP8, 64kbit density with I2C I/F in a SOP8, 256kbit density with SPI I/F in a SOP8 and 256kbit density with parallel I/F in a TSOP28 package.

ROHM Semiconductor

www.rohm.com/eu

Cool white LED modules

with luminous flux up to 1740 lm

Vishay Intertechnology released three cool white LED modules assembled with 6 or 12 highbright LEDs. The VLPCo601A2 features 6 LEDs in a row on a 240x14mm PCB that provides 870 lm. The VLPC1201A2J features 12 LEDs in a row on a 240x14 mm PCB that provides

1740lm. The VLPC1201A2 is simply half a VLPC1201A2J, resulting in two modules each measuring 120X14mm 1740 lm, 5000K - 7000K with 6 LEDs

and luminous flux of 870lm. This broad portfolio of options allows designers to select the ideal size PCB and light intensity for their applications. Designed to replace fluorescent lights in commercial, industrial, and residential applications, for

backlighting signage, and for automotive applications, the VLPCo601A2, VLPC1201A2J, and VLPC1201A2 offer a colour temperature range of 5000 K to 7000 K. The devices feature a shiny white surface and a metal-core, single-side PCB with a Cu thickness greater than 0.75 µm. The

> VLPCo601A2 features an LED pitch of 40 mm while the VLP-C1201A2J and VLPC1201A2 have an LED pitch of 20 mm. All three mod-

ules have a maximum current of 700mA and viewing angle of ± 80°. All are based on InGaN technology. The LED modules are available in colour bins. Vishay Intertechnology

www.vishay.com

DESIGN PRODUCTS

Highly efficient power inductors

rated at 20A for automotive applications

TDK-EPC Corporation has developed the VLM13580-D1 and DR SMD power inductors for use as choke coils in the DC-DC converters of automotive engine control units (ECU). The VLM13580-D1 and DR series can now be used at a temperature range from -40 to +150 °C. The use of a ferrite core with low loss and improved DC superimposition characteristics achieves much higher efficiency. The VLM13580T-2R2M-D1 is rated

at 20 A (maximum) versus 15 A (maximum) of

the existing VLM10555T-2R5M8R0-2H types. The product lineup comprises eight components (six D1 products and two DR products) with various inductances.

TDK-EPC Corporation

www.tdk.co.jp



highly linear for use in MRI medical instrumentation

Peregrine Semiconductor's PE4141 broadband quad MOSFET array core features low conversion loss of 5.8 dB, high linearity at 25 dBm, and



isolation of 44 dB at 100 MHz (LO to IF and RF to IF), making it suitable for low-frequency mixer applications. The array operates with differential signals at all ports

(RF, LO, IF), which makes it possible to de-

velop an analog multiplexer that uses LO ports as digital controls, and RF and IF ports as singleended or differential inputs/outputs. The device also supports up conversion or down conversion

in mixer applications.

Peregrine Semiconductor

www.psemi.com

Solderless LED socket

for Bridgelux RS LEDs

TE Connectivity added the RoHS-compliant Type BR socket for quick termination of Bridgelux RS LEDs to its line of solderless LED sockets. The socket eliminates the need to design, manufacture and integrate a complex metal clad printed circuit board assembly into a lighting fixture. Additionally, it provides lighting designers

with a broad range of LED mounting options

as it can be easily positioned and assembled anywhere

in a fixture using simple hand tools.

TE Connectivity

www.te.com/lighting

Wireless stereo audio modules

feature audio codec firmware update

Laird Technologies has released its enhanced Bluetooth BTM510/511and BTM520/521 wireless stereo audio modules with new firmware update. The firmware comes already loaded on all new modules and includes features such as supporting digital audio via an I2S bus and supporting universal General Purpose Input/Output (GPIO) functions for mapping GPIOs to specific Audio/Video Remote Control Profile (AVRCP) functions. The firmware includes a license free version of CSR's

aptX audio codec technology for Bluetooth stereo audio quality. Using non-destructive coding techniques, CSR's aptX audio codec for Bluetooth A2DP preserves the full "wired" audio quality of stereo transmitted over the 2.4 GHz ISM band from Laird Technologies' BTM510/511and BTM520/521 wireless modules, each of which integrates an audio DSP.

Laird Technologies

www.lairdtech.com



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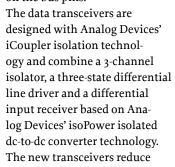
RS-485 data transceivers

5-kVrms signal and power isolated

011

Analog Devices, Inc., has introduced the ADM2682E and ADM2687E, the industry's first single-chip 5-kVrms signal- and power-isolated RS-485 data transceivers that meet the safety isolation requirements of high

voltage systems in motor, power and energy control systems. The new data transceivers also feature ±15kV ESD protection on the bus pins.



component count by up to 80 percent compared to discrete competitive options. Packaged in a single 10 mm x 13 mm surface mount package with greater than 8 mm minimum creepage and clearance, the transceivers

> occupy 70% less board space than the multiple discrete components typically used. The ADM2682E and ADM2687E

achieve data rates of 16 Mbps and 500 kbps, respectively. The new isolated transceivers are powered by a single 5-V or 3.3-V supply and integrate a 5-kVrms isolated dc-to-dc converter, which eliminates the need for an external dc-to-dc isolation block. **Analog Devices**

www.analog.com

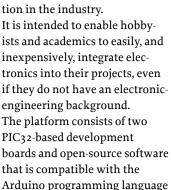
1110

Arduino-compatible 32bit MCU

delivered in open-source development platform

Microchip Technology and Digilent have co-launched the first 32bit microcontrollerbased, open-source development platform that is compatible with Arduino hardware and software. Designed and manufactured by Digilent, Microchip's authorised

design partner, the chipKIT platform is claimed to be the first and only 32bit Arduino solu-



and development environment, thanks to the work done by Mark Sproul and Rick Anderson through Fair Use Building and Research Labs.

The chipKIT hardware is compatible with existing 3.3V Arduino shields and applica-

tions, and can be developed using a modified version of the Arduino IDE and existing Arduino re-

sources, such as code examples, libraries, references and tutorials. The platform provides an unprecedented level of features for the Arduino community, and four times the performance of any existing Arduino solution at a low price—the boards start at just \$26.95 each.

Microchip Technology

www.microchip.com

Potted power supply

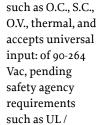
offers IP68 ingress protection

GlobTek's new GT-91120 series

of in-line power supplies offer double-enforced insulation mechanical configurations and regulated outputs voltage from 5 V to 48 Vdc in

o.1 V increments, up to 30 W of continuous output power. Style enclosed power supplies are potted in a 98.2x46.5x38.2 mm impact resistant polycarbonate case and feature thermal conduction cooling. The power supply family features a regulated output with low ripple as well

as built-in protection features



cUL 1950/60601.1 and TUV EN60950/60601.1. The device complies with EMI/RFI Regulations, EMC Directives/ CE and FCC Class B for ITE/medical applications.

GlobTek

SlobTek

www.globtek.co.uk

Low on-resistance power MOSFETs

drive up vehicle electrical efficiency

Better energy efficiency as well as size and cost benefits are what STMicroelectronics promises for customers of its extended line of STripFET VI DeepGATE power MOSFETs. The chipmaker

has added nine new automotivegrade devices to the product line. The new power transistors aim at applications in comfort, body

and power-train electronics. Energy-efficient electrical systems are increasingly important to car makers. These systems manage equipment from window winders, wipers and heater blowers to engine controllers, starter-alternators and energy recovery systems. Hybrid and electric vehicles, especially, need effective energy management for maximum traveling range. ST's new power MOSFETs will minimize the energy normally lost in electrical drives and controls, leading to greater efficiency, while simultaneously reducing heat generation, allowing smaller, more lightweight

assemblies. This new series of AEC-Q101-qualified 30 V and 40 V power devices uses ST's STrip-FET VI DeepGATE technology to achieve very low conduction losses relative to their active chip

size. They feature low on-resistance ranging from 3.0 milliohms up to 12.5 milliohms in industrystandard DPAK or D2PAK



surface-mount power packages, taking up less board space. This new range of power MOSFETS also includes both logic- and standard-level types. To assure reliability and robustness for automotive-grade applications, all devices undergo 100% avalanche testing both at wafer level and as finished products to meet the conditions for AEC-Q101 qualification. The new devices will also increase the efficiency of power supplies and drives for a wide range of non-automotive equipment and applications.

STMicroelectronics

www.st.com

DESIGN PRODUCTS

Avnet Abacus and FCI sign partnership

to address special connector needs

Distributor Avnet Abacus and connector maker FCI are launching a joint Europe-wide initiative aimed at helping designers choose the right connector for demanding applications in the industrial market. Renewable energy, Machine-to-Machine (M2M) interfacing and industrial control systems are typical examples of the demanding applications market segments that pose particular design and manufacturing challenges.

"FCI is fully committed to supporting



Avnet Abacus and FCI

www.avnet.com



as storage, displays & boards division

Rutronik Elektronische Bauelemente GmbH has now integrated Discomp, a fully-owned subsidiary, into the parent company. The Discomp operations will extend the "Displays & Embedded Boards" division in Rutronik to form a new division, named "Storage, Displays & Boards", under the leadership of former Director Discomp Frank Bittigkoffer.

"Storage, Displays & Boards" is composed of

two separate product groups: the "Storage" group, which will continue to be managed by Waldemar Batke, concerns itself with storage systems, including memory modules, flash memories, magnetic and optical disk drives, while "Displays & Boards", under the management of Michael Eger.

www.rutronik.com

Rutronik Elektronische Bauelemente

Marl extends low-cost LED portfolio

with high-intensity white devices up to 3W

LED components distributor Marl Optosource has extended its range of competitively priced LEDs in a number of colours and configurations, including high-intensity 1W and 3W white LEDs, further surface-mount and through-hole devices, and RGB LEDs for indoor applications.

The latest additions to Marl's Ledman portfolio are manufactured in China, and prove their high quality credentials by achiev-

ing ultra-high reliability and lumen maintenance figures better than

50ppm failures and 5% luminance degradation after up to 6000 hours testing.

Marl Optosource

www.optosource.com

1kHz counter timers

in a 47.9x34x54.5mm package

The Anly H₇E from specialist distributor Switchtec offers users valuable monitoring facilities in control panels and other equipments where lapsed time or events have to recorded. The H7E is available as two variants to cover specific tasks. The H7E-C is an 8-digit totalising counter, and the H7E-T is a 7-digit timer counter.

The H7E-C has the option for standard (30Hz nominal) counting, and using a built in DIP switch can be converted to high speed

1kHz counting. It can count up to 999,999,999. The

H₇E-T hours run counter display can be switched between hours and minutes or hours, minutes and seconds, again via the built in DIP switch. It can count up to 9999h 59.9m or 999h 59m 59s.

Switchtec

www.switchtec.co.uk





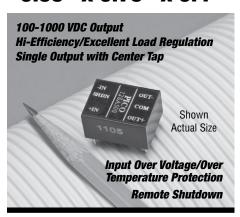
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Head in the clouds?

By Graham Curren

THERE HAS BEEN a lot of talk lately about the benefits of accessing EDA tools hosted in the cloud. In fact in most industries it's hard to avoid talk of the cloud and the improvements it can have on both productivity and general running costs for businesses. However the EDA industry is being held back by outdated licensing agreements and by tools that were not conceived with the cloud in mind.

As with any application, the software needs to be designed for the method in which it is used or else it becomes clunky, awkward and ultimately ineffective. If you're trying to access anything from off site, whether that's in the cloud or just working remotely, there will always be a delay in accessing and then processing data – anyone who has worked remotely using a VPN will appreciate this.

When you're working on complex and large files this problem becomes more than just an inconvenience. For those involved in full custom layout work or even design planning, things must be able to move smoothly across the screen or it becomes unworkable. The challenge for EDA vendors is to develop tools that take this into account; while batch work can be tackled effective remotely, interactive work needs fast screen response times and, today, this is only possible with locally hosted machines. In the future, by developing the application with this in mind, it may be possible to overcome this restriction.

The multiprocessor side of EDA is poor at present (although the EDA vendors would no doubt disagree), so there's a lot of work to be done before the benefits of cloud processing can be realised. This will become more apparent when jobs can run across a hundred or even thousand different CPUs, which may be running multiple jobs; something massive data centres can offer. But this sort of parallelism is currently not supported by the tools.

The advantage of working in the cloud is that you've got access to a massive warehouse full of the latest and quickest proces-

Graham Curren is CEO of Sondrel – www.sondrel.com – he can be reached on graham.curren@sondrel.com

sors. This is an advantage whether you're an SME working on your first few designs or a publicly traded company looking to speed up tape-out.

From the tool vendors' point of view there's little motivation in allowing someone to do a job in a minute when they can take a hundred using a single CPU on their own site and have to pay more licensing — and this brings us onto the other big issue with EDA in the cloud — EDA licensing.



"The EDA industry is being held back by outdated licensing agreements and by tools that were not conceived with the cloud in mind."

Some vendors, including Synopsys and Cadence, have previously offered cloud services, but they have yet to take off in a big way and one reason for that is because engineering teams can't be restricted to just one vendor (no vendor has a full best in class tool

suite today and arguably, apart from Synopsys, all have big holes). Therefore what's needed is a third party to host multiple vendor tools. The question then becomes, who is paying for the license and at what stage?

It's ultimately up to the EDA vendors to resolve this, but it does mean they will have to change the current business model. They will need to embrace licensing a tool to somebody for it to then be licensed again, across the cloud to someone they don't know – and that's what they don't like.

Aside from it not fitting with existing business models there's no real reason why vendors couldn't adopt a pay as you go approach, but currently there's nobody willing to take on the task of getting agreement for this. The only companies with the corporate weight to make this happen are the likes of Google or Amazon, but it's hard to see them getting into what is, for them, a pretty select market.

Security is also always going to be a fear for those looking to adopt cloud based services and while many of these fears are very understandable, the majority are just down to a fear of the new and unknown. People are already used to sending data off-site, whether this is to the foundries for tape-out or to the EDA companies themselves for debugging. However sending your new product RTL to Amazon carries a different risk, in that it's not a tried and tested approach.

The odd thing with this is that while businesses may have a dedicated on-site server room, their security levels both on the network and physically will likely pale in comparison to the data centres of Amazon or Google. Security will always be an issue, but nearly all of these concerns are manageable and not a genuine obstacle to working in the cloud.

I believe that working in the cloud can have numerous benefits for any company, even in the EDA space. However, so far, no attempts have taken off and I don't believe they will until someone takes on the role of hosting and, more importantly, getting the EDA vendors to agree to new licensing models. This is the biggest hurdle EDA faces to ever working in the cloud and sadly there is no sign of it changing in the near term.





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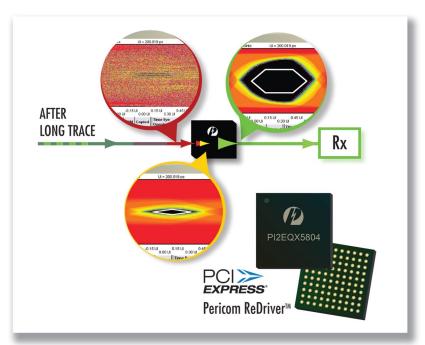




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